

## Pin Description

No.	Pin No	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	GND connectable
2	A3	Power	D	VDDLSC	1.1 V power supply
3	A4	Power	D	VDDMIO	1.8 V power supply
4	A5	Power	D	VDDMIO	1.8 V power supply
5	A6	Power	D	VDDLSC	1.1 V power supply
6	A7	Power	D	VDDLCN	1.1 V power supply
7	A8	—	—	N.C.	GND connectable
8	A9	O	A	VRHT	Capacitor connection
9	A11	—	—	N.C.	GND connectable
10	B3	GND	D	VSSLSC	1.1V GND
11	B4	GND	D	VSSLSC	1.1V GND
12	B5	GND	D	VSSLSC	1.1V GND
13	B6	GND	D	VSSLSC	1.1V GND
14	B7	GND	D	VSSLCN	1.1V GND
15	B8	—	—	N.C.	GND connectable
16	B9	GND	A	VSSHPX	2.9V GND
17	C1	Power	D	VDDLIF	1.1 V power supply
18	C2	GND	D	VSSLSC	1.1V GND
19	C3	—	—	N.C.	GND connectable
20	C4	O	A	TVMON	TEST output pin, OPEN
21	C5	—	—	N.C.	GND connectable
22	C6	—	—	N.C.	GND connectable
23	C7	—	—	N.C.	GND connectable
24	C8	—	—	N.C.	GND connectable
25	C9	—	—	N.C.	GND connectable
26	C10	GND	A	VSSHPX	2.9V GND
27	C11	O	A	VRLRS	Capacitor connection
28	D1	GND	D	VSSLSC	1.1V GND
29	D2	GND	D	VSSLSC	1.1V GND
30	D3	—	—	N.C.	GND connectable
31	D4	GND	A	VSSHAN	2.9V GND
32	D5	GND	A	VSSHPX	2.9V GND
33	D6	GND	A	VSSHPX	2.9V GND
34	D7	GND	A	VSSHPX	2.9V GND
35	D8	GND	A	VSSHPX	2.9V GND
36	D9	—	—	N.C.	GND connectable
37	D10	GND	A	VSSHPX	2.9V GND
38	D11	O	A	VRLT	Capacitor connection
39	E1	O	D	DMO3N	CSI-2 output (data)
40	E2	O	D	DMO3P	CSI-2 output (data)
41	E3	—	—	N.C.	GND connectable
42	E4	Power	A	VDDHAN	2.9 V power supply
43	E5	Power	A	VDDHAN	2.9 V power supply
44	E6	Power	A	VDDHPX	2.9 V power supply
45	E7	Power	A	VDDHPX	2.9 V power supply
46	E8	Power	A	VDDHPX	2.9 V power supply

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47	E9	—	—	N.C.	GND connectable
48	E10	—	—	N.C.	GND connectable
49	E11	—	—	N.C.	GND connectable
50	F1	O	D	DMO1N	CSI-2 output (data)
51	F2	O	D	DMO1P	CSI-2 output (data)
52	F10	GND	D	VSSLSC	1.1V GND
53	F11	Power	D	VDDLSC	1.1 V power supply
54	G1	GND	D	VSSLSC	1.1V GND
55	G2	GND	D	VSSLSC	1.1V GND
56	G10	I	D	TENABLE	Test enable, OPEN
57	G11	Power	D	VDDMIO	1.8 V power supply
58	H1	O	D	DCKN	CSI-2 output (clock)
59	H2	O	D	DCKP	CSI-2 output (clock)
60	H10	I	D	SLAMODE0	Select slave address
61	H11	I	D	XCLR	System clear
62	J1	GND	D	VSSLSC	1.1V GND
63	J2	GND	D	VSSLSC	1.1V GND
64	J10	I	D	SLAMODE1	Select slave address
65	J11	I/O	D	SDA	Serial data communication
66	K1	O	D	DMO2N	CSI-2 output (data)
67	K2	O	—	DMO2P	CSI-2 output (data)
68	K3	—	—	N.C.	GND connectable
69	K4	—	—	N.C.	GND connectable
70	K5	Power	A	VDDHAN	2.9 V power supply
71	K6	—	—	N.C.	GND connectable
72	K7	Power	A	VDDHPX	2.9 V power supply
73	K8	Power	A	VDDHPX	2.9 V power supply
74	K9	—	—	N.C.	GND connectable
75	K10	I/O	D	SCL	Serial clock input
76	K11	I/O	D	XVS	Vertical sync signal
77	L1	O	D	DMO4N	CSI-2 output (data)
78	L2	O	D	DMO4P	CSI-2 output (data)
79	L3	—	—	N.C.	GND connectable
80	L4	—	—	N.C.	GND connectable
81	L5	GND	A	VSSHXP	2.9V GND
82	L6	—	—	N.C.	GND connectable
83	L7	GND	A	VSSHXP	2.9V GND
84	L8	GND	A	VSSHXP	2.9V GND
85	L9	—	—	N.C.	GND connectable
86	L10	I/O	D	TOUT	Digital TEST output pin, OPEN
87	L11	I/O	D	XHS	Horizontal sync signal
88	M1	GND	D	VSSLSC	1.1V GND
89	M2	GND	D	VSSLSC	1.1V GND
90	M3	—	—	N.C.	GND connectable
91	M4	—	—	N.C.	GND connectable
92	M5	—	—	N.C.	GND connectable
93	M6	—	—	N.C.	GND connectable
94	M7	—	—	N.C.	GND connectable
95	M8	—	—	N.C.	GND connectable

No.	Pin No	I/O	Analog / Digital	Symbol	Description
96	M9	—	—	N.C.	GND connectable
97	M10	GND	D	VSSLSC	1.1V GND
98	M11	I	D	INCK	Master clock input
99	N3	GND	D	VSSLSC	1.1V GND
100	N4	GND	A	VSSLPL2	1.1V GND
101	N5	GND	A	VSSLPL1	1.1V GND
102	N6	GND	D	VSSLSC	1.1V GND
103	N7	GND	D	VSSLSC	1.1V GND
104	N8	GND	D	VSSLSC	1.1V GND
105	N9	GND	D	VSSLCN	1.1V GND
106	P1	—	—	N.C.	GND connectable
107	P3	Power	D	VDDLIF	1.1 V power supply
108	P4	Power	A	VDDLPL2	1.1 V power supply
109	P5	Power	A	VDDLPL1	1.1 V power supply
110	P6	Power	D	VDDLSC	1.1 V power supply
111	P7	Power	D	VDDMIO	1.1 V power supply
112	P8	Power	D	VDDLSC	1.1 V power supply
113	P9	Power	D	VDDLCN	1.1 V power supply
114	P11	—	—	N.C.	GND connectable