SMT-EW10x/30x Series Tuner Module Application Note

Version 0.2.0.0

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Revision History

Version	Date	Note
0.1.0.0		
0.2.0.0	06, Apr., 2015	Added channel scan function (Chapter.6) Added DVB-T2 PER function (Section 7.1.15)

Contents

1. Overview

SMT-EW10x and EW30x series are tuner modules designed for receiving the DVB-T2, DVB-T, and ISDB-T broadcasting.
SMT-EW10x is a single solution tuner module, and EW30x supports 2-diversity reception to improve mobility performance.
This document will describe detailed function of the SMT-EW10x and EW30x series tuner module and how to control the tuner module using with I2C, SPI or SDIO host bus interfaces.

1.1. Block Diagram

Following shows the block diagram of the SMT-EW10x and EW30x tuner module.
The tuner module can be controlled via the I2C (SDA/SCL), SPI (SS/SCK/MISO/MOSI) or SDIO (SDIO_CLK/CMD/DT0~3) host interface selected by SPI_SEL and SDIO_SEL pin configuration (See the “Host Interface” section).
TS packets are output from TS I/F port (TSDATA/TSCLOCK/TSVALID/TSPSYNC), SPI or SDIO port.
If user choose the I2C bus for tuner control, I2C slave address needs to be configured by ADR0 and ADR3 (See next section).

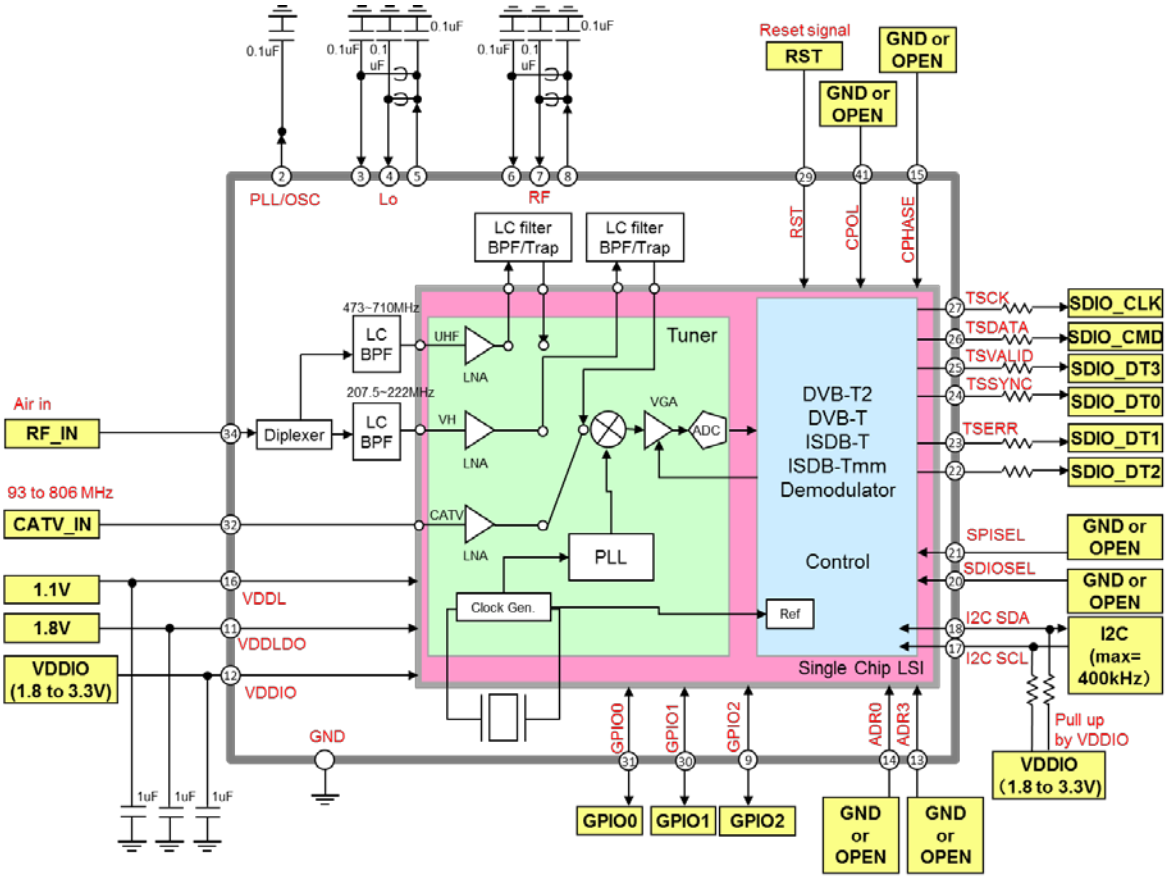
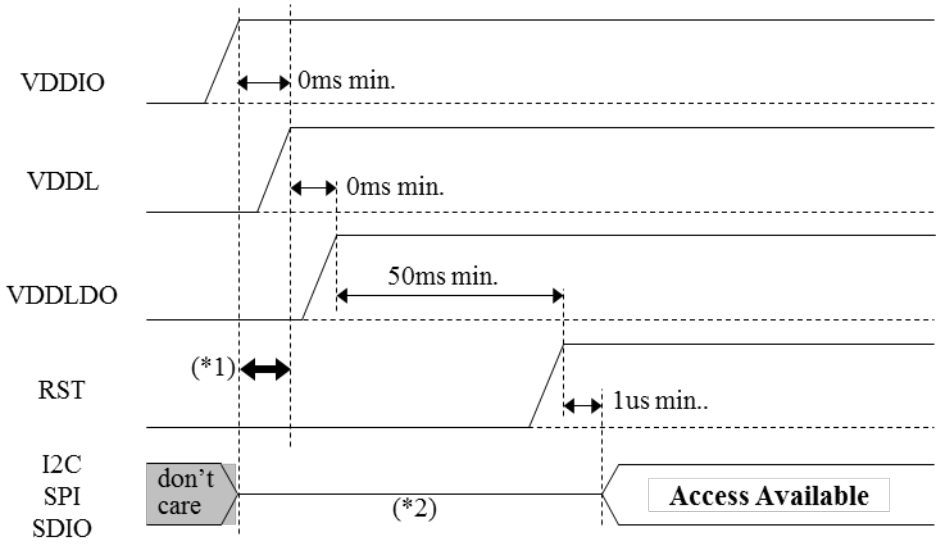


Fig. 1-1 SMT-EW10x Block Diagram

1.2. Power and Reset Sequence

At tuner boot process, following power supply and reset signal sequence are required.

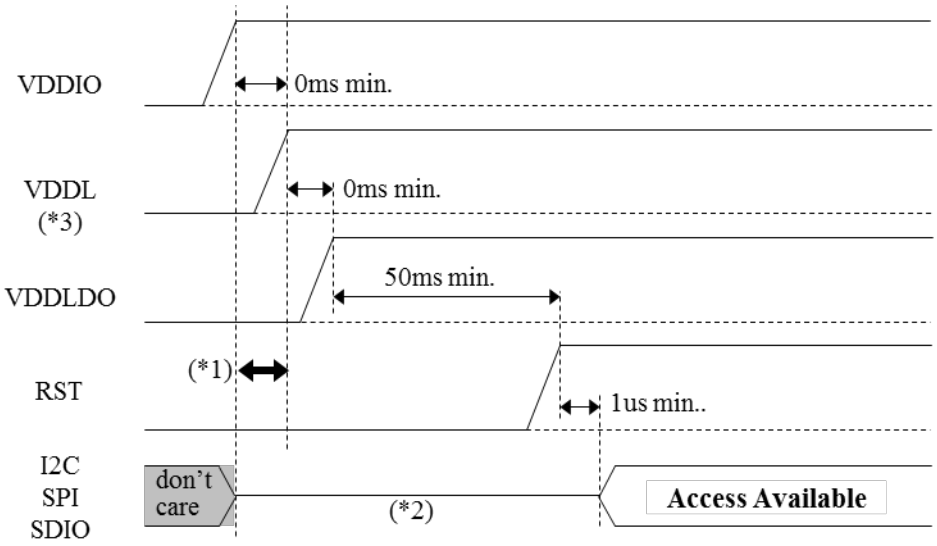
- Internal LDO Mode



(*1) Gated I/O mode: The term of only VDDIO is "High"
(*2) During this term, any devices' control are not allowed accessing.

Fig. 1-2 Power Sequence for Internal LDO Mode

- External LDO Mode



(*1) Gated I/O mode: The term of only VDDIO is "High"
(*2) During this term, any devices' control are not allowed accessing.
(*3) At "External LDO Mode", VDDL needs to be connected with VDDRF, VDDRF2, VDDIF, VDDLO0, VDDLO1, VDDLO2, and VDDPLL/OSC.

Fig. 1-3 Power Sequence for External LDO Mode

2. Host Interface

The tuner module can be controlled via the I2C, SPI or SDIO host interface selected by 'SPI_SEL' and 'SDIO_SEL' pin configuration like following table.

Table 2-1 SMT-EW10x/EW30x Host I/F selection

SDIOSEL	SPISEL	I2C Control	SPI Control	SDIO Control
0	0	**Available**	Not Available	Not Available
0	1	Not Available	**Available**	Not Available
1	0	Not Available	Not Available	**Available**
1	1	**Available**	Not Available	Not Available

2.1. Register structure

Fig.2-1. shows register structure in the SMT-EW10x and EW30x. Both tuner and demodulator block has a bank structure, with 256 banks and 256 register addresses per a bank. Address from 0x00 to 0x0F are assigned to special registers shared by all banks. Address from 0x10 to 0xFF are assigned to normal registers which are switched by the bank number setting. The register of register address 0x00 is used to specify the bank number.

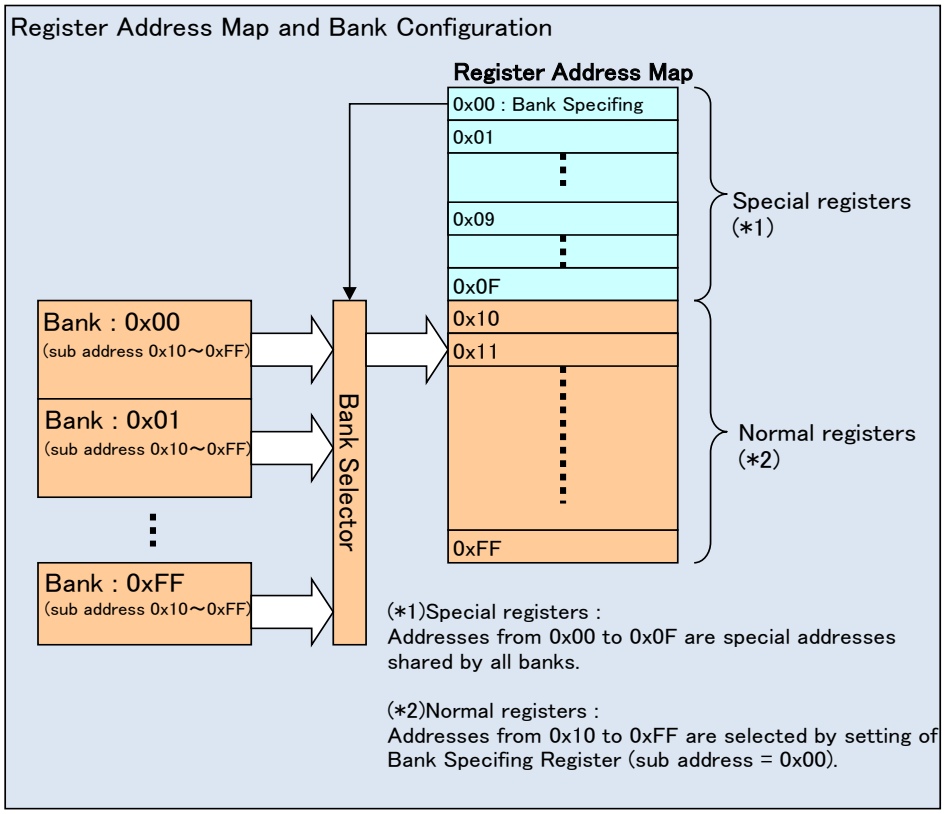


Fig. 2-1 I2C Register Bank Configuration

For example, the access method for a Bank 0x01 register of demodulator by I2C interface is shown below.

【Register setting example】

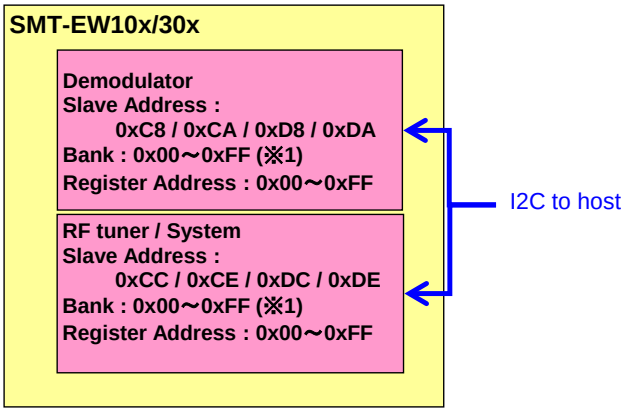
I2C	Slave Address	Bank	Register Address	Data
Write	0xD8	0x01	0x6A	0x50

Step 1) Write Data 0x01 to Register address 0x00 in order to change bank to 0x01
I2C write sequence : (Slave Address:0xD8, Register address:0x00, Data:0x01)

Step 2) Set Data 0x50 to Bank 0x01, Register address 0x6A by writing Data 0x50 to Register address 0x6A after Step 1)
I2C write sequence : (SlaveAddress:0xD8, Register address:0x6A, Data:0x50)

2.2. I2C Interface

I2C control diagram is shown in Fig.2-2.
This tuner module supports both I2C Standard mode(100kHz) and Fast mode(400kHz).



(※1) The I2C register of Demodulator Block has a bank configuration,
with an address space of 256 banks, and 256 words (1 word = 8 bits) per b

Fig. 2-2 I2C Control Diagram

I2C slave address needs to be configured by ADR0 and ADR3. Slave address of each block is shown in a following table.

Table 2-2 SMT-EW10x/30x I2C slave address table

SLVADR3	**1**		**1**		**0**		**0**	
SLVADR0	**0**		**1**		**0**		**1**	
	Write	Read	Write	Read	Write	Read	Write	Read
Demod	0xD8	0xD9	0xDA	0xDB	0xC8	0xC9	0xCA	0xCB
SYSTEM (RF)	0xDC	0xDD	0xDE	0xDF	0xCC	0xCD	0xCE	0xCF

I2C data format is as follows.

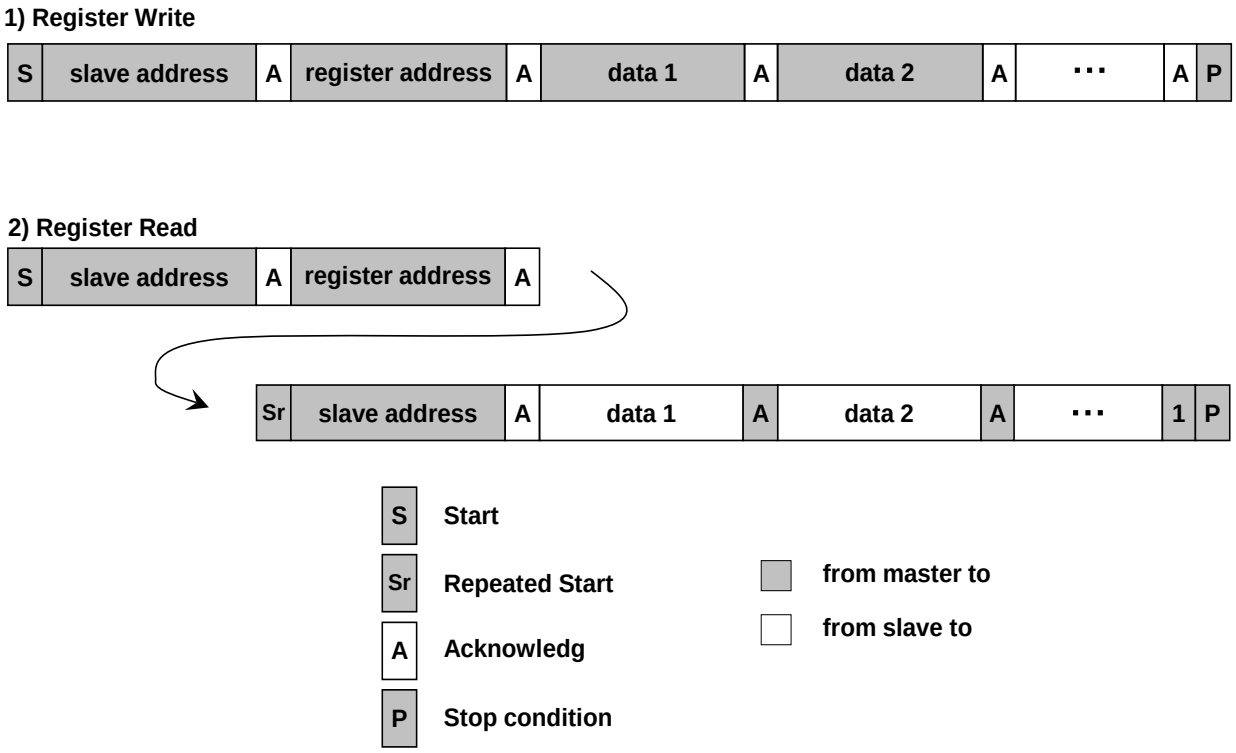
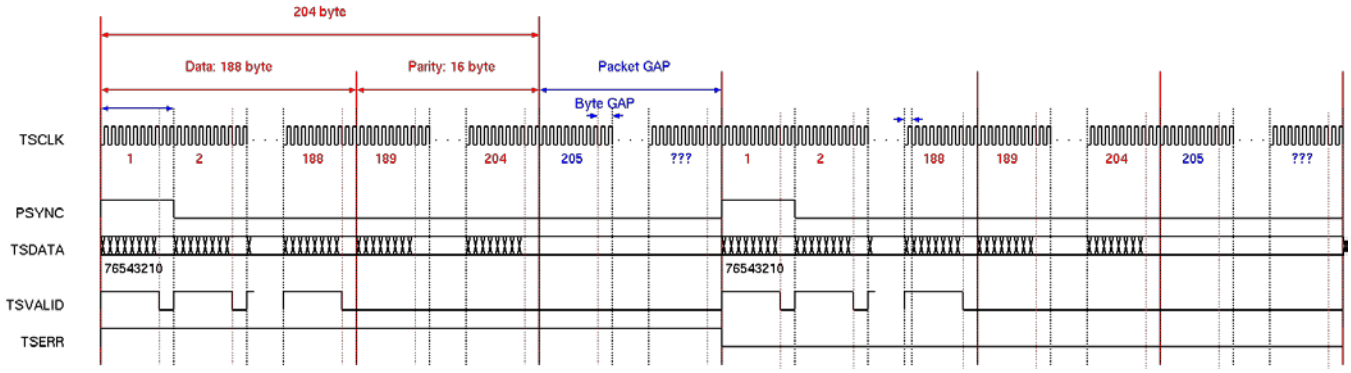


Fig. 2-2 Demodulator I2C Write / Read Format

2.3. TS Interface

2.3.1. TS output format

SMT-EW10x/30x series tuner module supports DVB-SPI compliant TS output format. Following shows a typical DVB-SPI TS timing chart.



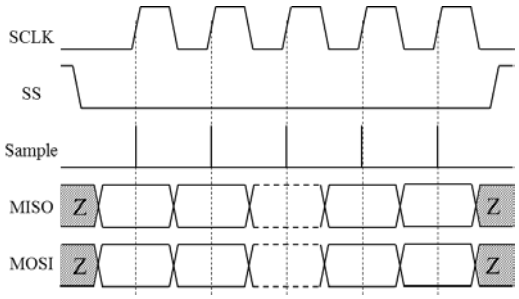
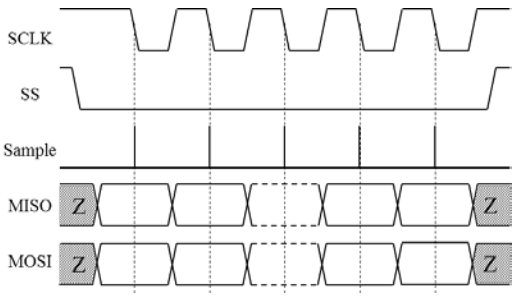
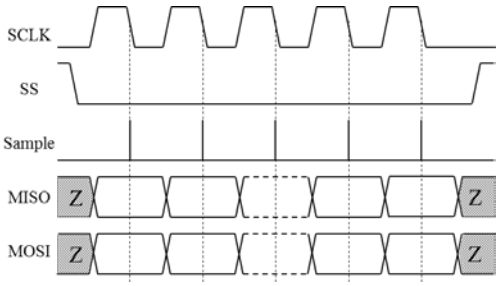
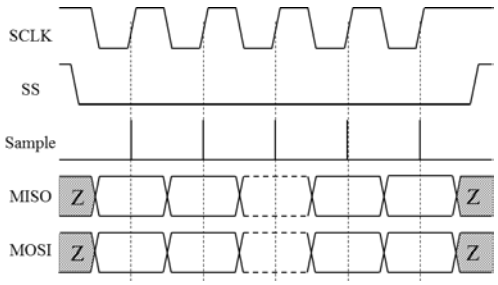
TSCLK frequency can be selected to Full-rate mode or Half-rate mode by register configuration, and also TSCLK/TVALID format, parity packet gap can be configured as following examples. For more detailed register setting, please see later chapter.

2.4. SPI Interface

By setting SPISEL pin “H” and SDIOSEL pin “L”, tuner internal register can be controlled by SPI interface. Also, TS data can be read via this interface.

2.4.1. SPI transfer mode

In case using SPI control, 4 types mode can be selected by “CPHASE” and “CPOL” pin condition as following figure.

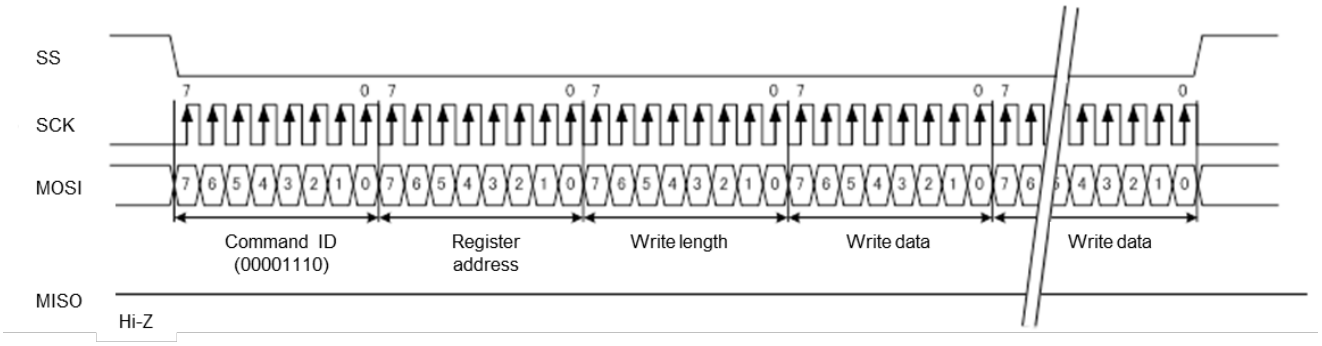
	CPOL = 0	CPOL = 1
CPHASE = 0		
CPHASE = 1		

2.4.2. Tuner register control function

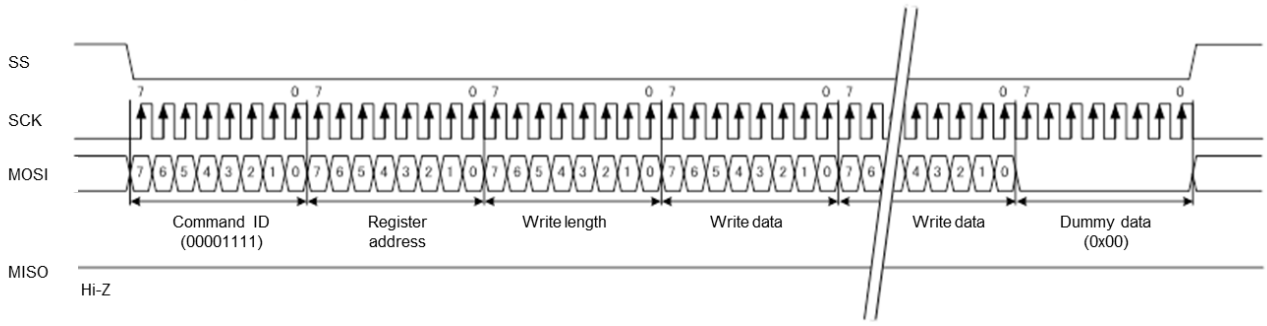
To read or write the tuner internal register, following SPI commands are defined.
Each command ID is 1byte long, and need register address and length information as command arguments.

Function	Command ID	Arguments	Response	Description
Write Demod. Register	00001110	Register address Number of write bytes	N/A	Write data to demodulator register (see following Ex.1 for detail)
Write RF Register	00001111	Register address Number of write bytes	N/A	Write data to RF register (see following Ex.2 for detail)
Read Demod. Register	00001010	Register address Number of read bytes	Read data	Read data from demodulator register (see following Ex.3 for detail)
Read RF Register	00001011	Register address Number of read bytes	Read data	Read data from RF register (see following Ex.3 for detail)

➢ Ex.1) Data format for writing demodulator register

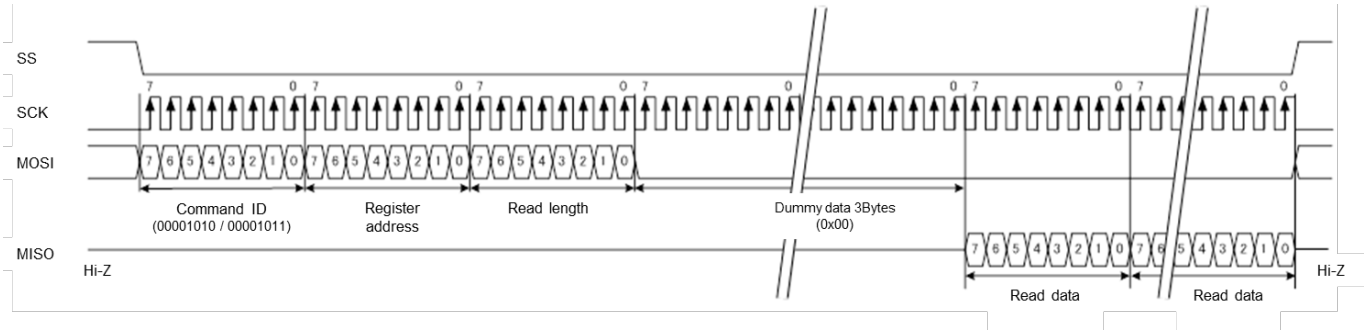


➢ Ex.2) Data format for writing RF register
* When writing to RF register, 1byte dummy data is needed.



➢ Ex.3) Data format for reading register

* Register data start to be read 4byte(Read length + 3byte dummy data) after sending register address.

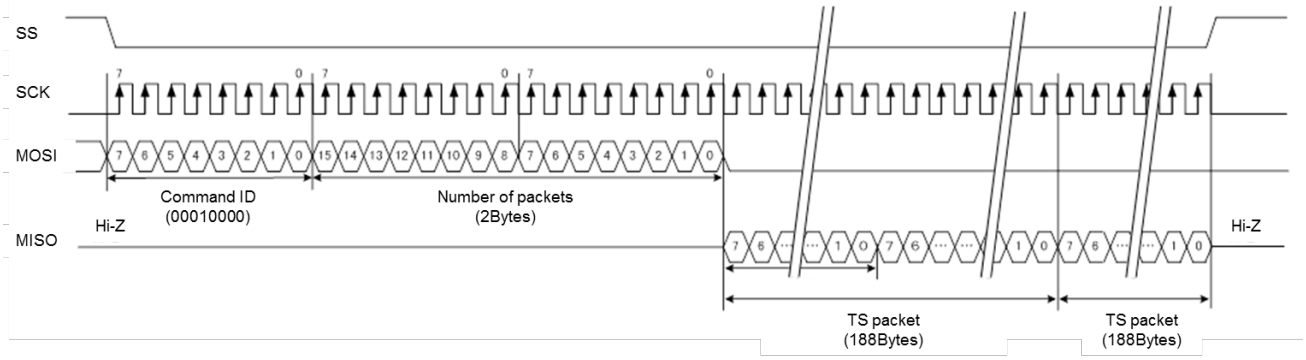


2.4.3. TS read and buffer control function

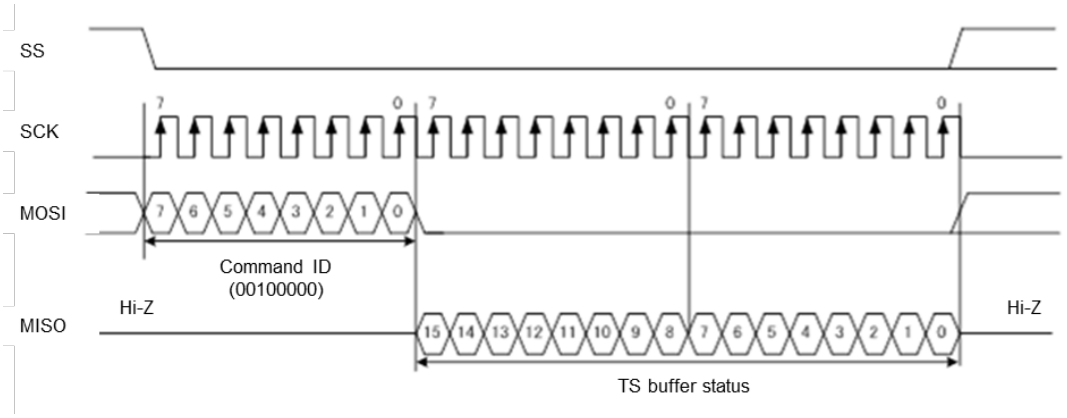
User can read TS data, and TS buffer status by using following SPI commands.
And also, TS buffer can be cleared by SPI command if necessary.

Function	Command ID	Arguments	Response	Description
Read TS	00010000	Number of read packets	TS data	Read TS data by 1packet unit (see following Ex.4 for detail)
Read status	00100000	N/A	Buffer status	Read TS buffer status (see following Ex.5 for detail)
Read status / TS	00110000	Number of read packets	TS data and buffer status	Read both TS buffer status and TS data (see following Ex.6 for detail)
Buffer clear	00000011	N/A	N/A	Clear TS buffer (see following Ex.7 for detail)

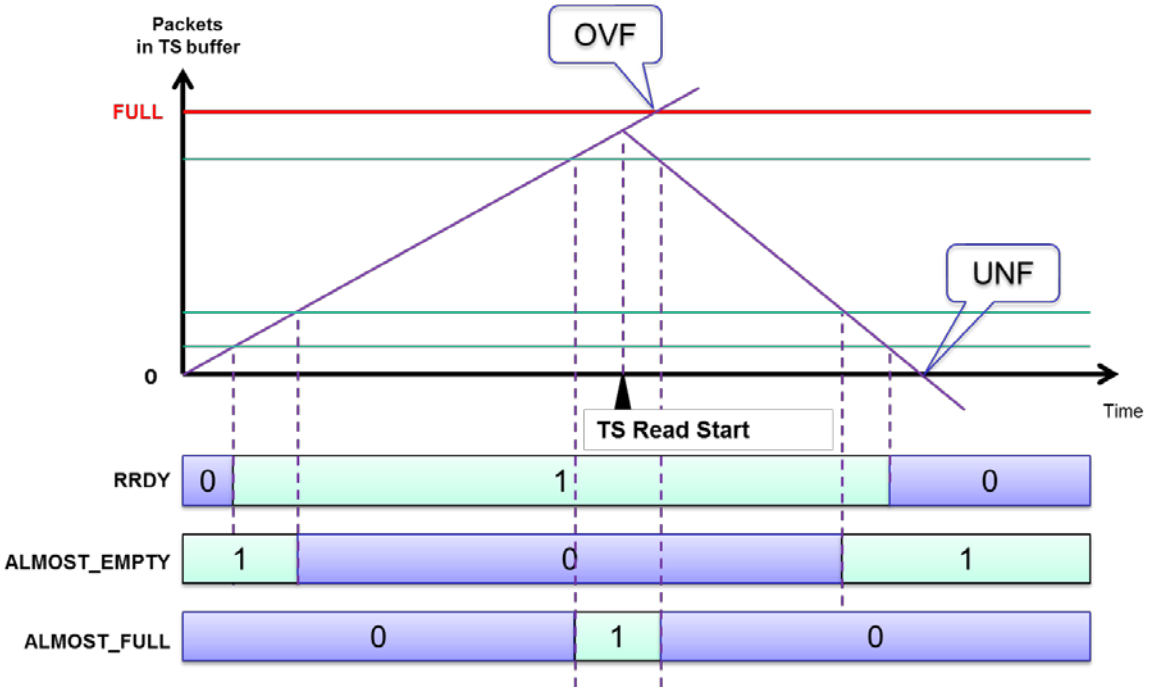
➢ Ex.4) Data format for reading TS packets



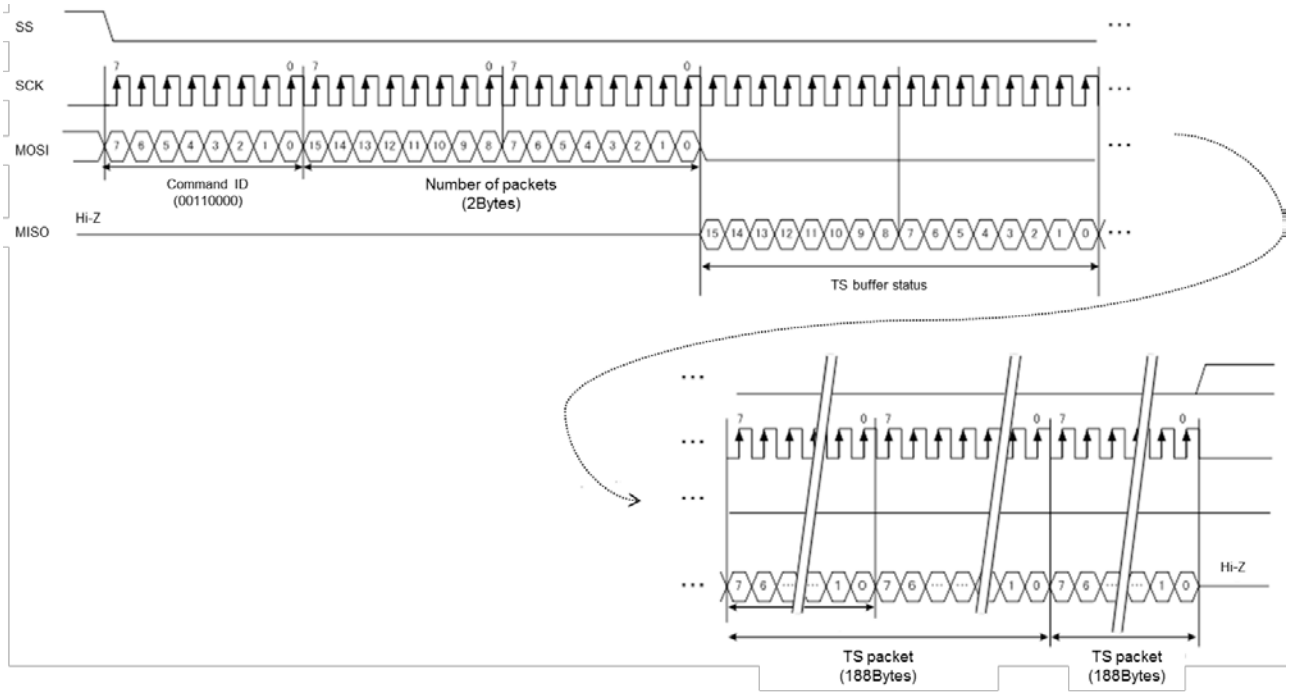
➢ Ex.5) Data format for reading TS buffer status



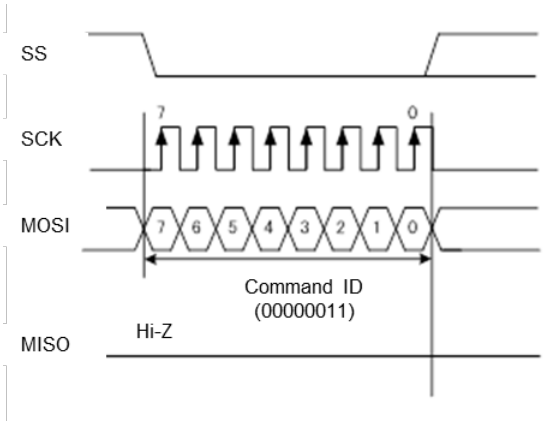
Bit	Signal	Description
[15]	BUF_RRDY	TS buffer ready flag. If this bit is 1, TS data can be read from the TS buffer.
[14]	BUF_ALMOST_FULL	TS buffer almost full flag. If this bit is 1, TS data buffer is almost full.
[13]	BUF_ALMOST_EMPTY	TS buffer almost empty flag. If this bit is 1, TS data buffer is almost empty.
[12]	BUF_OVF	TS buffer overflow flag. If this bit is 1, TS buffer overflow occurred.
[11]	BUF_UNF	TS buffer underflow flag. If this bit is 1, TS buffer underflow occurred.
[10:0]	BUF_STORED_PKT	Number of packets in TS buffer.



➢ Ex.6) Data format for reading TS data and buffer status



➢ Ex.7) Data format of TS buffer clear command



2.5. SDIO Interface

By setting SPISEL pin “L” and SDIOSEL pin “H”, tuner internal register can be controlled by SDIO interface. Also, TS data can be read via this interface.

2.5.1. Supported SDIO command

SMT-EW10x/30x SDIO interface supports following SD mode commands. CMD52 and CMD53 are used to write/read registers and to read TS data.
Detailed description of each command type or response, please refer to the SDIO specification.

CMD INDEX	TYPE	RESPONSE	ABBREVIATION
CMD0	Broadcast command	-	GO_IDLE_STATE
CMD3	Broadcast command with response	R6	SEND_RELATIVE_ADDR
CMD5	SDIO command	R4	IO_SEND_OP_COND
CMD7	Addressed command	R1b	SELECT/DESELECT_CARD
CMD15	Addressed command	-	GO_INACTIVE_STATE
CMD52	SDIO command	R5	IO_RW_DIRECT
CMD53	SDIO command	R5	IO_RW_EXTENDED

2.5.2. Tuner register control function

To read/write to internal registers, SDIO CMD52 or CMD53 can be used. Both command can be used to access the register, but CMD52 is only for single byte read/write. If user want to use burst read or write, CMD53 should be used.

- CMD52 (Register Write)

S	D	Command index	R/W flag	Function number	RAW flag	Stuff	Register address	Stuff	Write data	CRC7	E
1	1	6	1	3	1	1	17	1	8	7	1
		110100b	1 (write)	1	0		Register address		Data to write		

- CMD52 (Register Read)

S	D	Command index	R/W flag	Function number	RAW flag	Stuff	Register address	Stuff	Write data	CRC7	E
1	1	6	1	3	1	1	17	1	8	7	1
		110100b	0 (read)	1	0		Register address		Stuff bits		

- CMD53 (Register Write)

S	D	Command index	R/W flag	Function number	Block mode	OP code	Register address	Byte/Block count	CRC7	E
1	1	6	1	3	1	1	17	9	7	1
		110101b	1 (write)	1	0 : Byte 1 : Block	0 : Fixed address 1 : Increment address	Register address	Data to write		

- CMD53 (Register Read)

S	D	Command index	R/W flag	Function number	Block mode	OP code	Register address	Byte/Block count	CRC7	E
1	1	6	1	3	1	1	17	9	7	1
		110101b	0 (read)	1	0 : Byte 1 : Block	0 : Fixed address 1 : Increment address	Register address	Stuff bits		

2.5.3. TS read and buffer control function

User can read TS data by using SDIO CMD53 as following.

- CMD53 (Register Read)

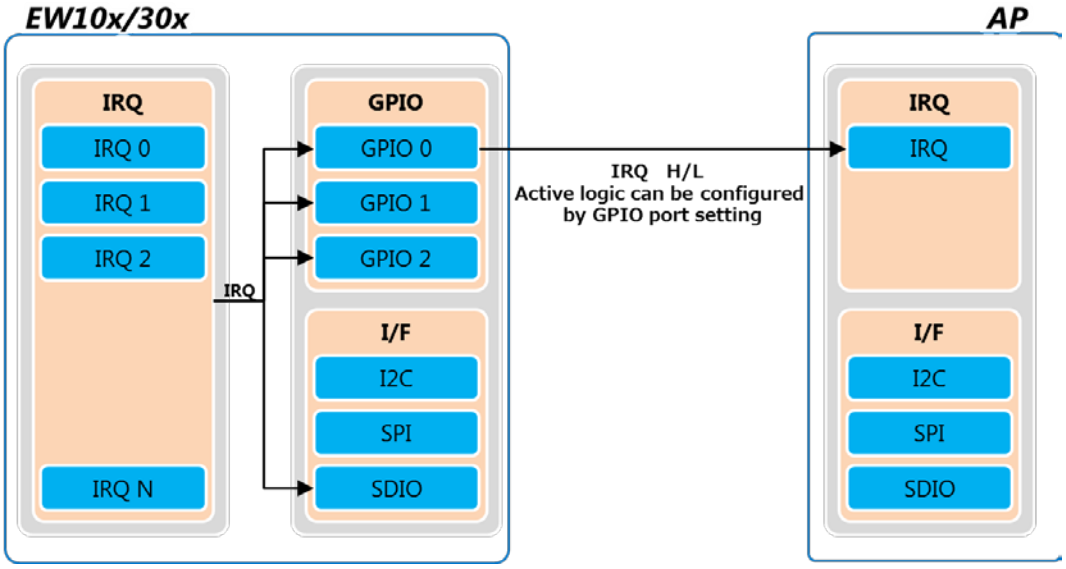
S	D	Command index	R/W flag	Function number	Block mode	OP code	Register address	Byte/Block count	CRC7	E
1	1	6	1	3	1	1	17	9	7	1
		110101b	0 (read)	1	1 : Block	0 : Fixed address	1_0000	N		

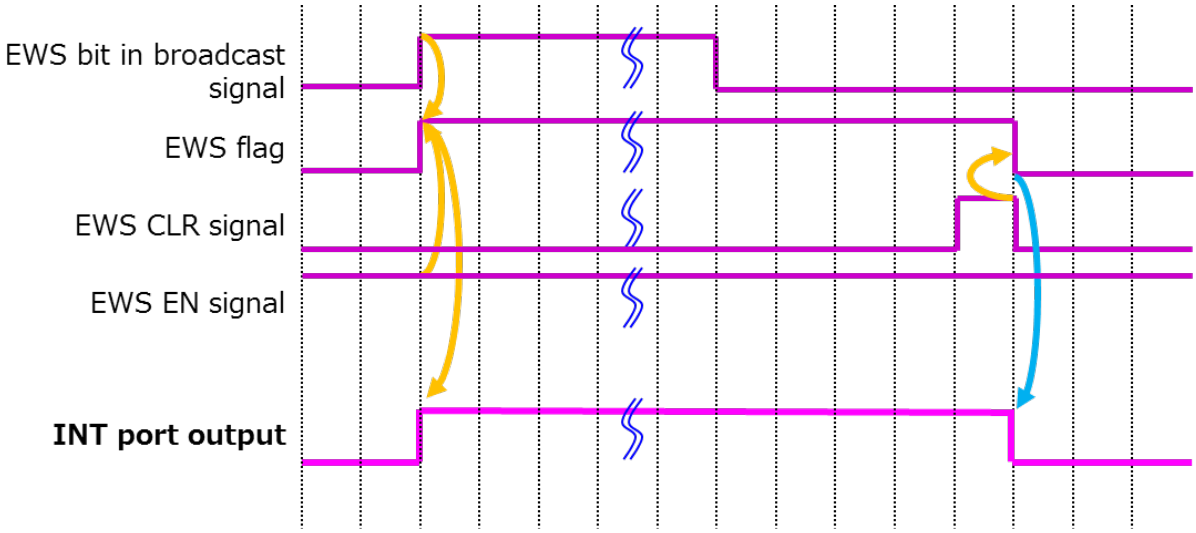
2.6. GPIO function

T.B.D.

2.7. Interrupt function

SMT-EW10x/30x tuner module can generate interrupt signal to the application processor to notify that tuner internal status changed. Interrupt related signal can be configured by tuner register setting, and the application processor can check the interrupt trigger signal by reading register after detecting “active” status of interrupt signal pin.
Interrupt output port can be selected from GPIO0~2 by register configuration.





Example operation of Interrupt (EWS signal trigger interrupt)

3. Control State Diagram

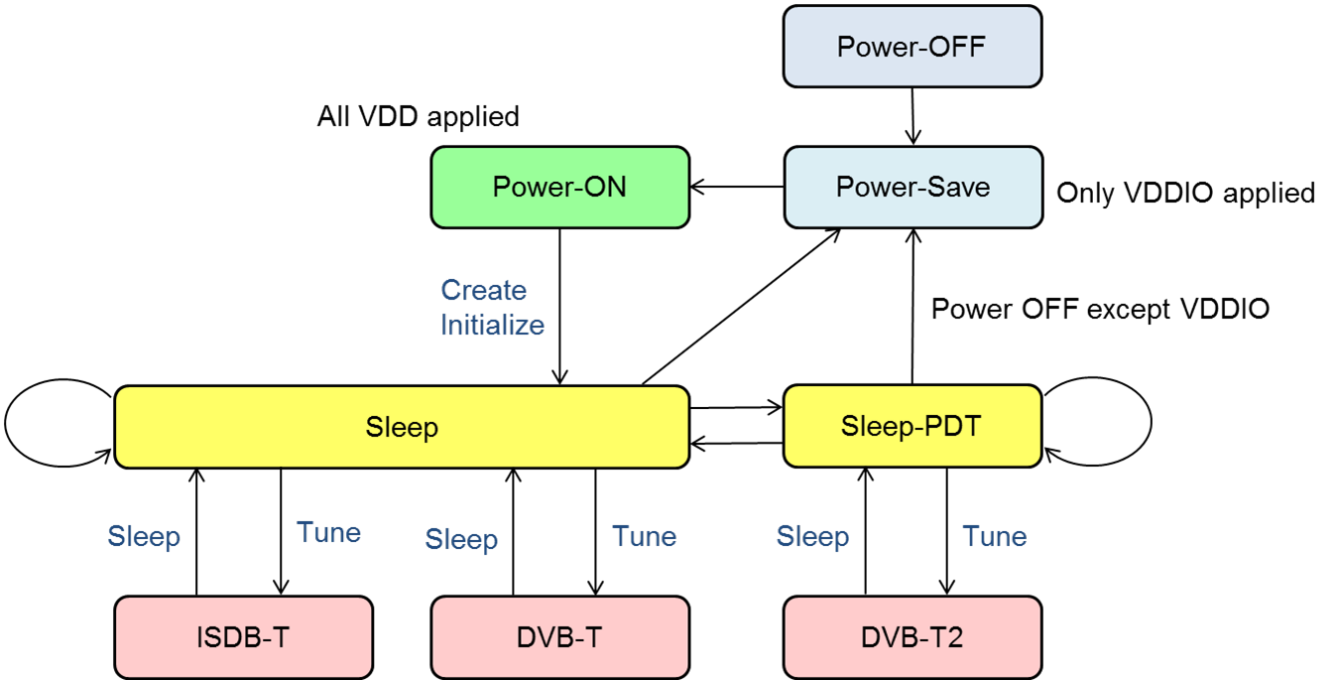
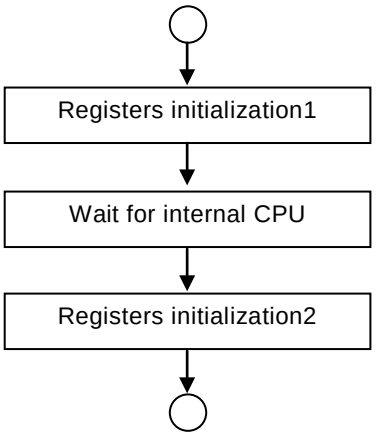


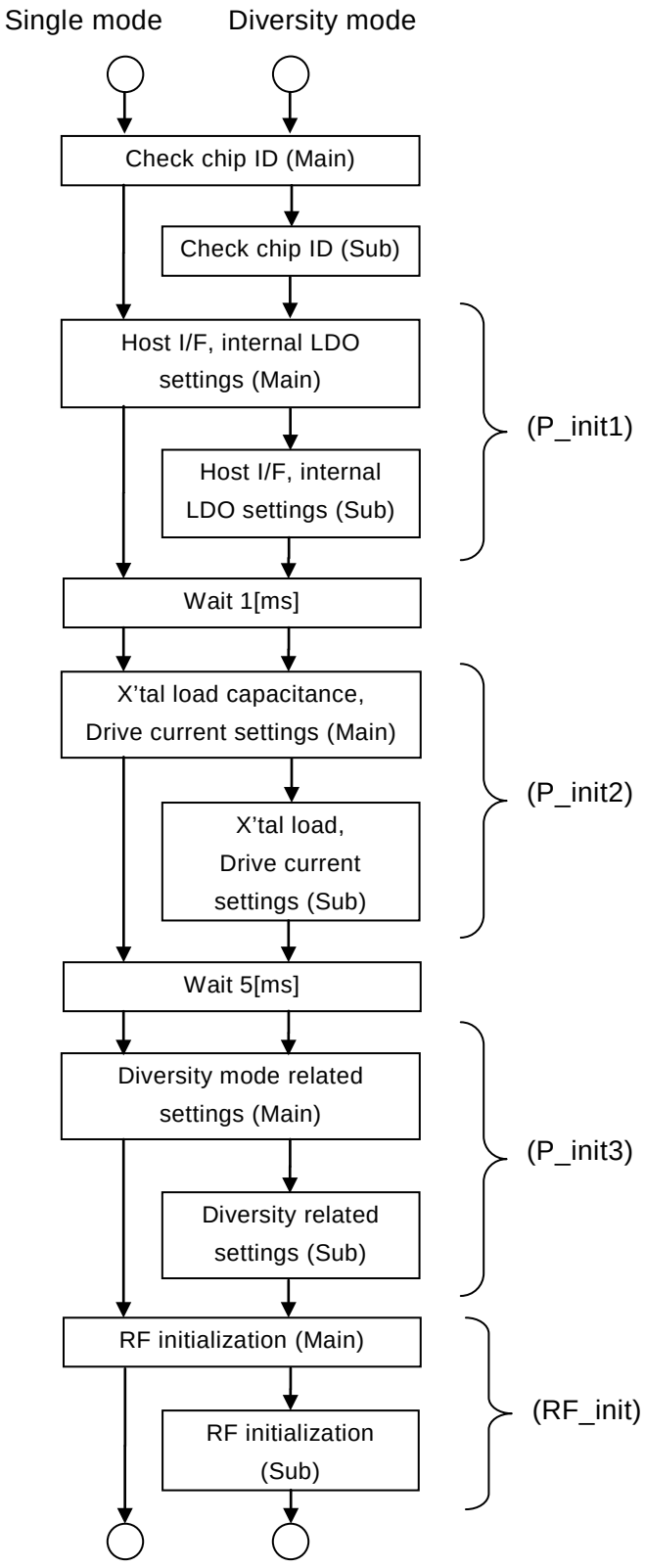
Fig. 3-1 SMT-EW10x/30x Control Flow

4. Initialization Flow

After all powers are turned on and hardware reset, tuner initialize process need to be performed.
This section describes the initialization process flow, and register settings.
Please also refer to “sony_integ_initialize()” function in the reference driver code.



4.1. Registers initialization1



4.1.1. Check chip ID

Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	System (RF)	0x00	0xFD	Chip ID	Chip ID 0x62: ES1.00, ES1.01 0x6A: ES1.11

4.1.2. P_init1

R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x10	Output I/F	Output I/F TS I/F : 0x00 SPI I/F : 0x01 SDIO I/F 0x02

Note : This setting is only for single tuner or diversity main tuner

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x11	0x16	
		0x10	0x10	data1	data1 If chip ID = 0x62 : 0x16 If chip ID = 0x64 : 0x1A
			0x11	LDO	LDO Internal LDO used : 0x01 Internal LDO NOTused : 0x00
			0x13	LDO	
		0x00	0x12	LDO	

4.1.3. P_init2

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x13	0x08	
			0x14	0x08	
			0x15	data1	data1, data2 Single reception : data1= 0x01, data2 = 0x01 Diversity main : data1= 0x00, data2 = 0x01 Diversity sub : data1= 0x01, data2 = 0x00
			0x16	data2	
			0x17	0x06	
			0x18	0x00	

4.1.4. P_init3

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x1F	data1	data1 Single reception : 0x00 Diversity main : 0x03 Diversity sub : 0x02
			0x20	0x01	

4.1.5. RF_init

Register R/W	Slave Address	Bank	Register Address	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
Write	System (RF)	0x00	0x21	0x01	0x00	0x01					
		0x10	0x17	0x01	0x01						
			0x4F	0x18							
			0x61	0x00							
			0x71	0x00							
			0x9D	0x01							
			0x7D	0x02							
			0x8F	0x01							
			0x8B	0xC6							
			0x9A	0x03							
			0x1C	0x00							
			0xB5	0x00	0x1F	0x0A					
			0xB9	0x07							
			0x33	0x01							
			0xC1	0x01							
			0xC4	0x1E							
			0xD9	0x2F	0x25	0x15	0x19	0x1B	0x15	0x19	0x1B
		0x11	0x44	0x6C	0x10	0xA6					
			0x50	0x16	0xA8						
			0x62	0x00	0x22	0x00	0x88				
			0x74	0x75							
			0x7F	0x05	0x05	0x05	0x05	0x05	0x05	0x05	0x05
			0x87	0x05	0x04	0x04	0x04	0x03	0x03	0x03	0x04
			0x8F	0x04	0x05	0x05	0x05	0x02	0x02	0x02	0x02
			0x97	0x02	0x02	0x02	0x02	0x02	0x03	0x02	0x01
			0x9F	0x01	0x01	0x02	0x02	0x03	0x04	0x04	0x04
		0x16	0x10	0x00	0x71						
			0x23	0x89							
			0x27	0xFF	0x00	0x00	0x00	0x00			
			0x3A	0x00	0x00	0x00	0x00	0x00	0x01	0x00	0x01
			0x42	0x00	0x02	0x00	0x63	0x00	0x00	0x00	0x03
			0x4A	0x00	0x04	0x00	0x04	0x00	0x06	0x00	0x06
			0x52	0x00	0x08	0x00	0x09	0x00	0x0B	0x00	0x0B
			0x5A	0x00	0x0D	0x00	0x0D	0x00	0x0F	0x00	0x0F
			0x62	0x00	0x0F	0x00	0x10	0x00	0x79	0x00	0x00
			0x6A	0x00	0x02	0x00	0x00	0x00	0x03	0x00	0x01
			0x72	0x00	0x03	0x00	0x03	0x00	0x03	0x00	0x04
			0x7A	0x00	0x04	0x00	0x06	0x00	0x05	0x00	0x07
			0x82	0x00	0x07	0x00	0x08	0x00	0x0A	0x03	0xE0
			0xBC	0x03	0xE0						
		0x10	0x51	0x01							
			0xC5	0x07							

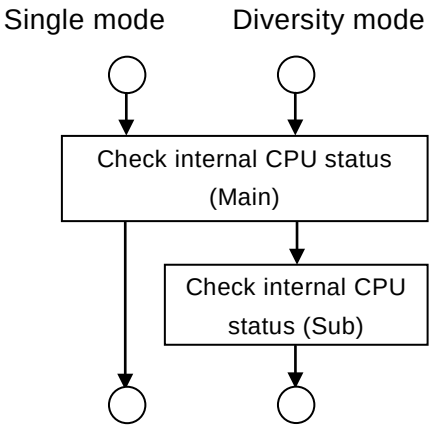
Register R/W	Slave Address	Bank	Register Address	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
Write	System (RF)	0x11	0x70	0xE9							
			0x76	0x04							
			0x78	0x2B							
			0x7A	0x3C							
			0x7C	0x77							
			0x7E	0x54							
		0x10	0xE1	0x01							
		0x12	0x10	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x16	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x1C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x22	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x28	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x2E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x34	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x3A	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x40	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x46	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x4C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x52	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x58	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x5E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x64	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x6A	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x70	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x76	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x7C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x82	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x88	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x8E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x94	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x9A	0x00	0x08	0x19	0x0E	0x09	0x0E		
		0x13	0x10	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x16	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x1C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x22	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x28	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x2E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x34	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x3A	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x40	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x46	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x4C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x52	0x00	0x08	0x19	0x0E	0x09	0x0E		

Register R/W	Slave Address	Bank	Register Address	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
Write	System (RF)	0x13	0x58	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x5E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x64	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x6A	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x70	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x76	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x7C	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x82	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x88	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x8E	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x94	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0x9A	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xA0	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xA6	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xAC	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xB2	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xB8	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xBE	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xC4	0x00	0x08	0x19	0x0E	0x09	0x0E		
			0xCA	0x00	0x08	0x19	0x0E	0x09	0x0E		
		0x11	0xBD	0x08	0x09						
			0xC4	0x08	0x09						
			0xC9	0x20	0x20	0x30	0x41	0x50	0x5F	0x6F	0x80
		0x14	0x10	0x15	0x18	0x00					
			0x15	0x00							
		0x16	0x12	0x00	0x09	0x00	0x08	0x00	0x07	0x00	0x06
			0x1A	0x00	0x05	0x00	0x03	0x00	0x02	0x00	0x00
			0x22	0x00	0x78	0x00	0x00	0x00	0x06	0x00	0x08
			0x2A	0x00	0x08	0x00	0x0C	0x00	0x0C	0x00	0x0D
			0x32	0x00	0x0F	0x00	0x0E	0x00	0x0E	0x00	0x10
			0x3A	0x00	0x0F	0x00	0x0E	0x00	0x10	0x00	0x0F
			0x42	0x00	0x0E						
Wait 1 [ms]											

Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	System (RF)	0x0A	0x10	data1	data1 If data1[0] == 0 : HW error happened
Write		0x00	0x25	0x00	
Wait 1 [ms]					
Read	System (RF)	0x0A	0x11	data2	data2 If data1[0] == 0 : HW error happened

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0x02	0x00	
			0x21	0x01	
		0xE1	0x8F	0x16	
			0x67	0x60	
			0x6A	0x0F	
			0x6C	0x17	
			0x6E	0x00	
			0x6F	0xFE	
			0x70	0xEE	
			0x8D	0xA1	
			0x8E	0x8B	
			0x77	0x08	
			0x78	0x09	
		0xE2	0x41	0xA0	
			0x4B	0x68	
		0x00	0x21	0x00	
			0x10	0x01	
	System (RF)	0x10	0x25	0x01	
Wait 1 [ms]					
Read	System (RF)	0x1A	0x10	data1	data1 If data1[0] == 0 : HW error happened
Write		0x10	0x14	0x01	
		0x00	0x26	0x00	

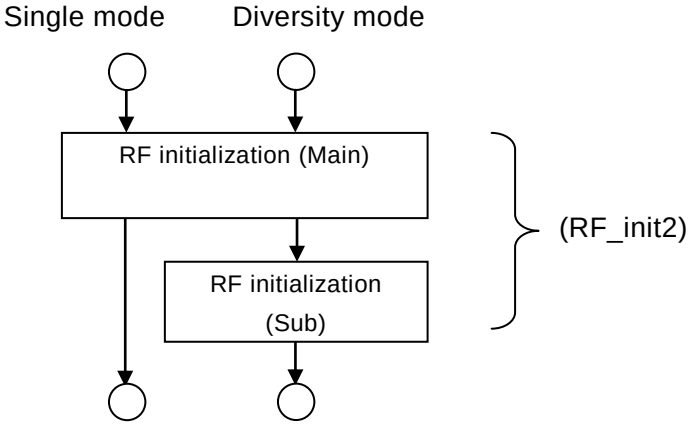
4.2. Wait for internal CPU



Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	System (RF)	0x1A	0x15	data1	CPU status = (data1 << 8) | data2 CPU status == 0x00 : Internal CPU is ready.
			0x16	data2	

(*) CPU calibration timeout is 500 [ms].

4.3. Registers initialization2

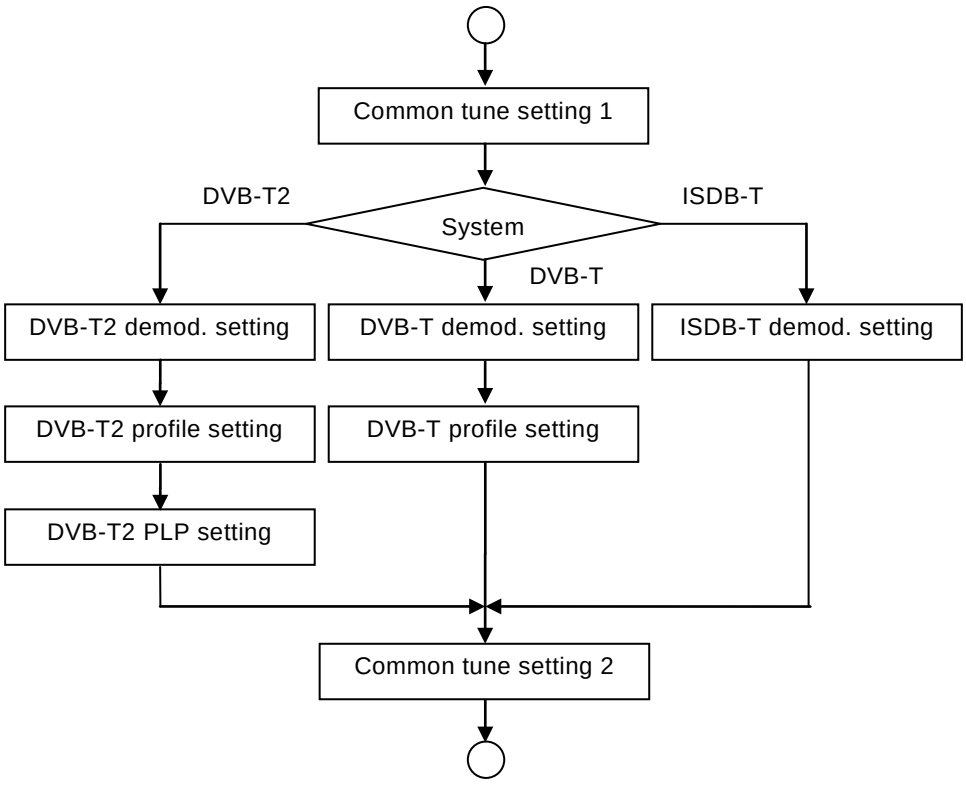


4.3.1. RF_init2

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x10	0xEA	0x40	
			0xEB	0x40	
Wait 1 [ms]					
Write	System (RF)	0x10	0x30	0x00	
			0x31	0x00	
			0x32	0x01	
			0x33	0x03	
		0x00	0x21	0x01	
		0xE1	0xD3	0x00	
		0x00	0x21	0x00	

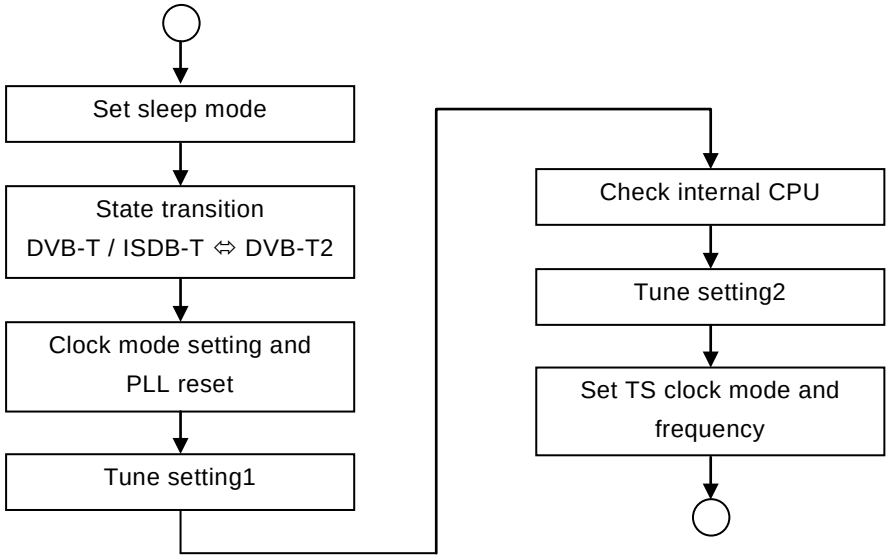
5. Tuning Flow

Following chart shows the SMT-EW100/300 DVB-T/T2, ISDB-T tuning process.
Tuning process consists of two major parts, common tune setting part and reception system dependent setting part. Following chart is simplified flow of tuning process. Detailed setting flow and register settings are described in later sections.
Please also refer to “sony_integ_dvbt2_Tune()”, “sony_integ_dvbt_Tune()”, and “sony_integ_isdbt_Tune()” function in the reference driver code.



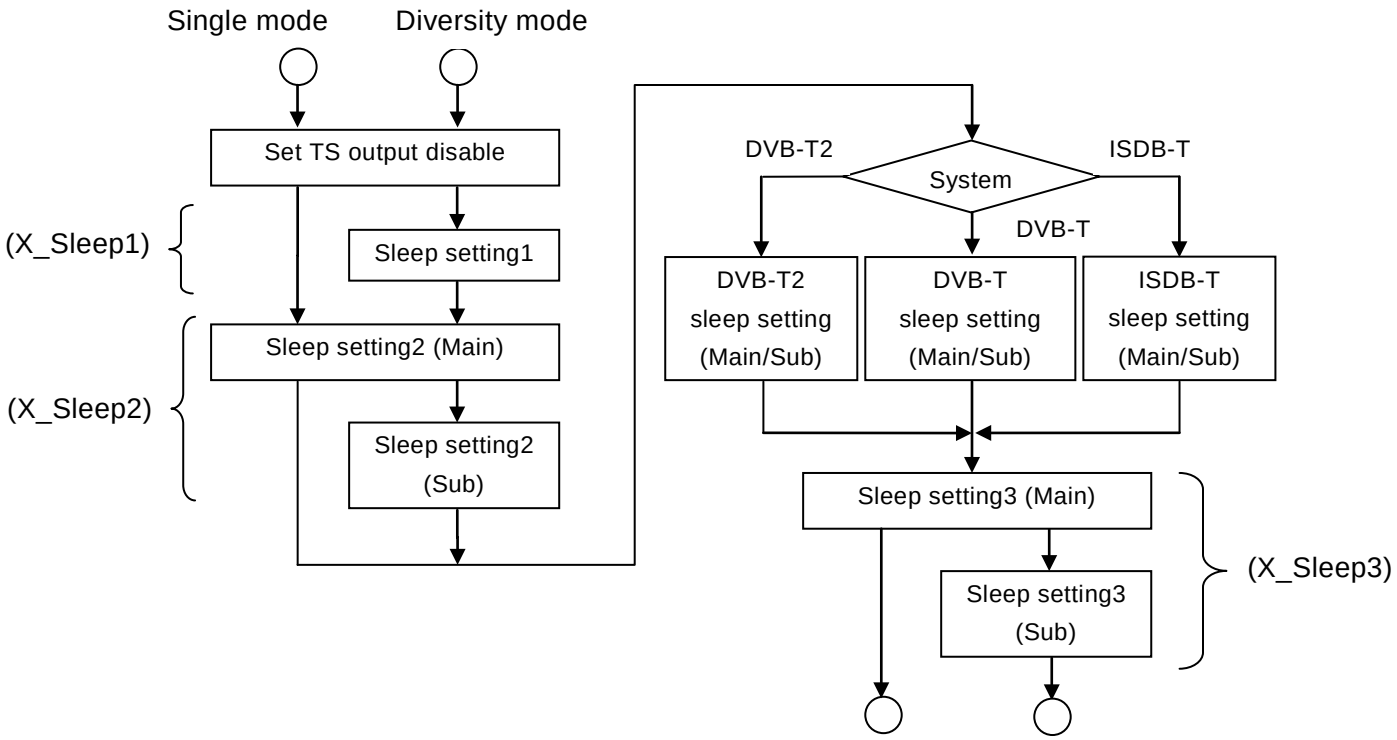
5.1. Common tune setting1

Following is flow of the first common tune settings. In this part, the tuner will be set to sleep mode, and then, DVB-T / ISDB-T ⇔ DVB-T2 state transition, clock mode setting, and some tuning setting will be done.



5.1.1. Sleep setting

At first, put the demodulator into sleep state.



5.1.1.1. TS output disable setting

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0xC3	0x01	TS output disable setting
	System (RF)	0x00	0x52	0x1F	

5.1.1.2. X_Sleep1

(For diversity main tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x57	0x03	
			0x53	0x00	
			0x54	0x00	

(For diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x55	0x1F	
			0x56	0xFF	
			0x57	0x03	
			0x53	0x00	
			0x54	0x00	

(For diversity main tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x55	0x1F	
			0x56	0xFF	

5.1.1.3. X_Sleep2

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x2D	0xB1	0x01	
Wait 1 [ms]					
Read	Demod.	0x2D	0xB2	data1	data1 If data1[0] == 0 : HW error happened
Write	System (RF)	0x10	0xF4	0x00	
			0xF3	0x00	
			0xF2	0x00	
			0xF1	0x00	
			0xF0	0x00	
			0xEF	0x00	

5.1.1.4. System dependent sleep setting

- For DVB-T2

  Noting to set.

- For DVB-T

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x04	0x5C	0xD8	

(Only for diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x11	0x87	0x04	

- For ISDB-T

Register R/W	Slave Address	Bank	Register Address	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
Write	Demod.	0x04	0x5C	0xD8							
			0x5E	0x00	0x14						
			0x72	0xB3	0x00	0xC4	0x5F	0x52	0x20	0x05	0x01
			0x7A	0x00	0x07	0x32					
			0x80	0x04	0x19	0x30	0x2D	0x04	0x06	0x0C	0x16
			0x88	0x04	0x08	0x10	0x00	0x00	0xFF	0x07	0xED
			0x90	0x46	0x07	0x00	0x00	0xFF	0x06	0xEF	0x36
			0x98	0x17	0x00	0x00	0x00	0x02	0xF7	0x1B	0x2C

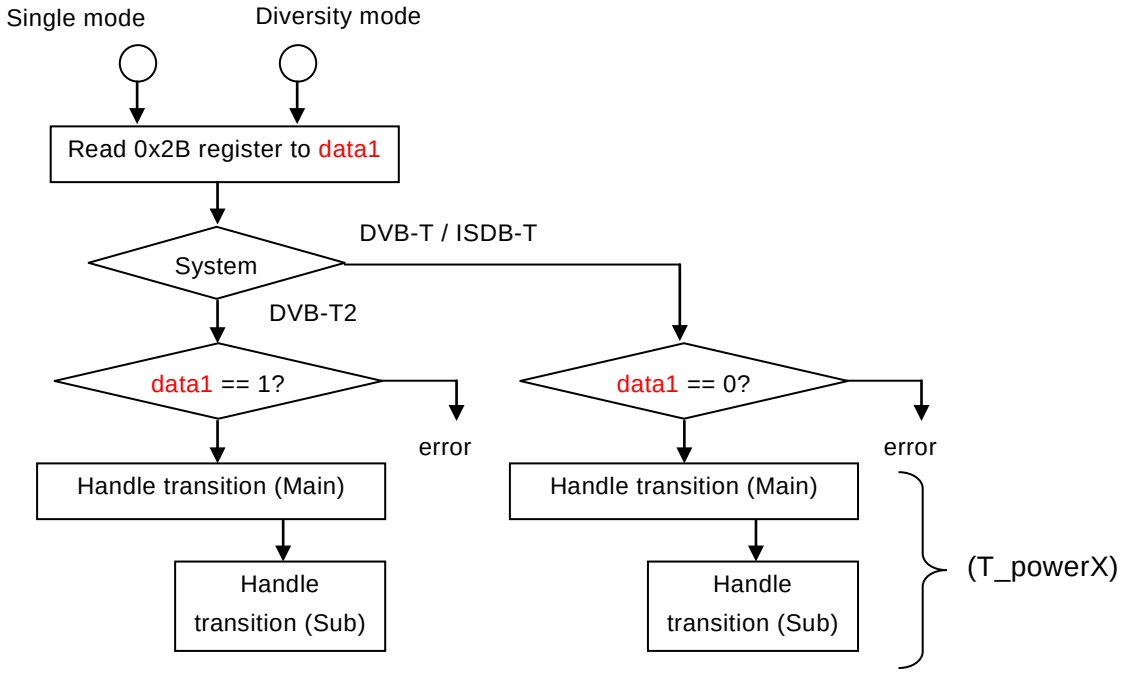
(Only for diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x10	0x94	0x04	

5.1.1.5. X_Sleep3

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0xFD	0x00	

5.1.2. State transition DVB-T/ISDB-T sleep ⇔ DVB-T2 sleep



Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	System (RF)	0x00	0x2B	data1	

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x10	0x29	0x01	
			0x28	0x01	
			0x27	0x01	
	Demod.	0x00	0x10	0x00	
	System (RF)	0x00	0x27	0x00	
			0x25	0x01	
System dependent setting (See following tables)					
Write	System (RF)	0x00	0x25	0x00	
Wait 1 [ms]					
Read	System (RF)	0x0A	0x11	data4	data4 If data1[0] == 0 : HW error happened
Write		0x00	0x27	0x01	
Wait 1 [ms]					
Write	System (RF)	0x00	0x10	0x01	
		0x10	0x27	0x00	
			0x28	0x00	
			0x29	0x00	

- System dependent setting (for DVB-T2)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x2A	0x03	
			0x2B	0x00	
Wait 1 [ms]					
Read	System (RF)	0x0A	0x13	data2	data2 If data1[0] == 0 : HW error happened

- System dependent setting (for DVB-T/ISDB-T)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x2B	0x01	
Wait 1 [ms]					
Read	System (RF)	0x0A	0x12	data3	data3 If data1[0] == 0 : HW error happened
Write		0x00	0x2A	0x00	

5.1.3. Clock mode setting

Clock mode will be decided following chart and tables.

Table S

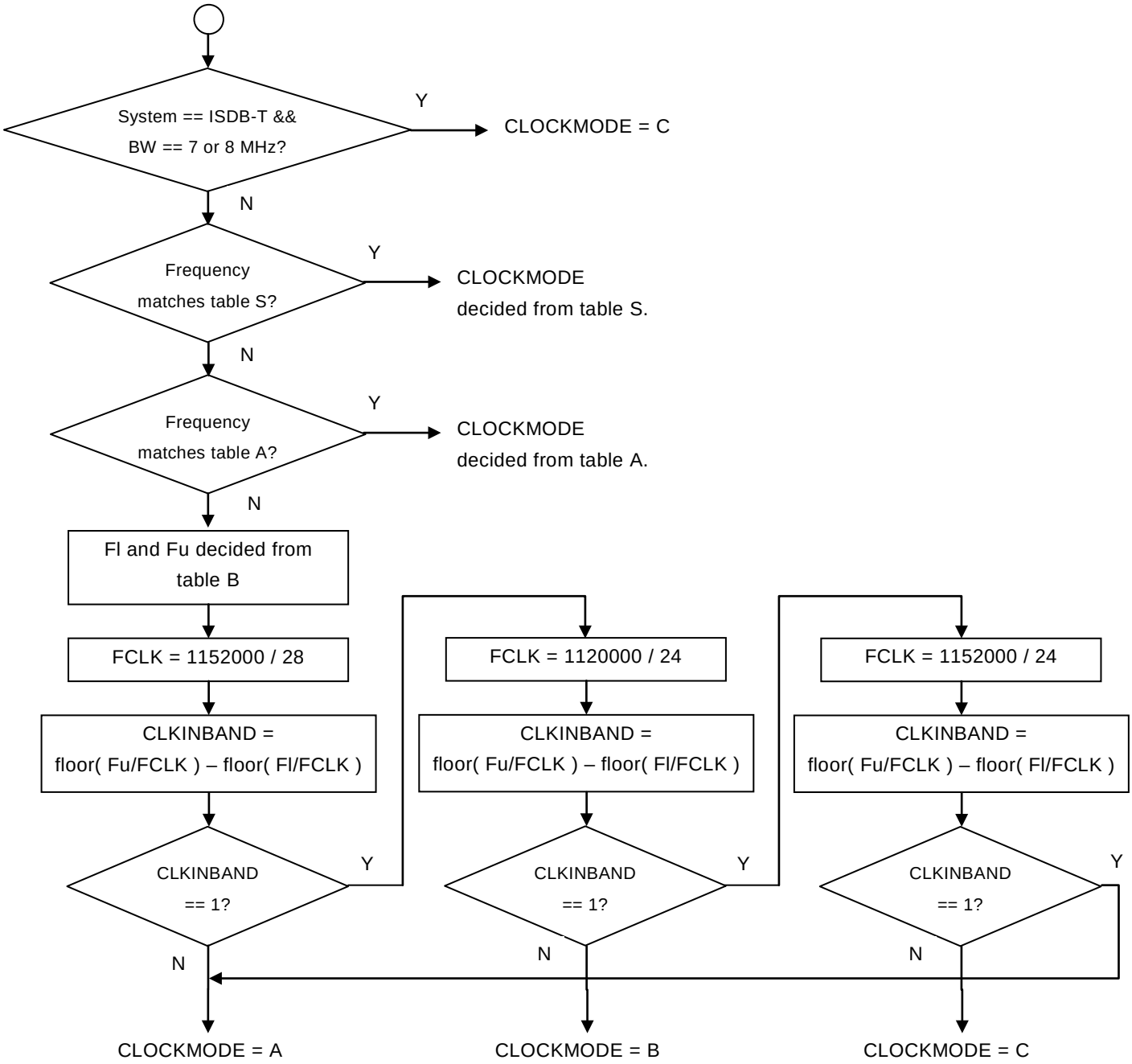
Freq (lower) [MHz]	Freq (upper) [MHz]	Clock mode
59.001	60.999	CLOCKMODE_B
86.501	88.499	CLOCKMODE_A
89.001	90.999	CLOCKMODE_B
119.001	120.999	CLOCKMODE_B
149.001	150.999	CLOCKMODE_B
174.001	175.999	CLOCKMODE_A
179.001	180.999	CLOCKMODE_B
209.001	210.999	CLOCKMODE_B
239.001	240.999	CLOCKMODE_B
349.001	350.999	CLOCKMODE_A
359.001	360.999	CLOCKMODE_B
479.001	480.999	CLOCKMODE_B
699.001	700.999	CLOCKMODE_C
719.001	720.999	CLOCKMODE_B

Table A

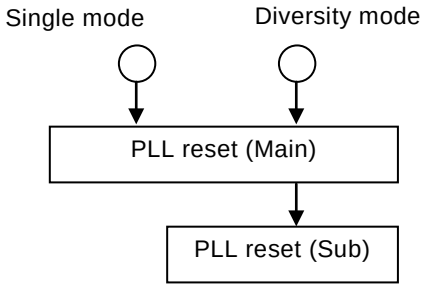
Freq (lower) [MHz]	Freq (upper) [MHz]	Clock mode
174.000	179.000	CLOCKMODE_A
179.001	226.499	CLOCKMODE_C
226.500	230.000	CLOCKMODE_A

Table B

BW [MHz]	Fu [kHz]	Fl [kHz]
1.7	f (RF) + 850	f (RF) - 850
5	f (RF) + 2500	f (RF) - 2500
6	f (RF) + 3000	f (RF) - 3000
7	f (RF) + 3500	f (RF) - 3500
8	f (RF) + 4000	f (RF) - 4000

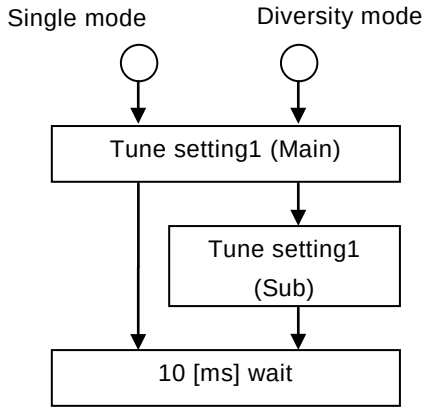


After changing clock mode, following PLL reset is needed.



Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x10	0x29	0x01	
			0x28	0x01	
			0x27	0x01	
			0x26	0x01	
	Demod.	0x00	0x10	0x00	
	System (RF)	0x00	0x27	0x00	
			0x22	0x01	
			0x30	data1	data1 CLOCKMODE_A : 0x00 CLOCKMODE_B : 0x01 CLOCKMODE_C : 0x02
			0x22	0x00	
Wait 2 [ms]					
Read	System (RF)	0x0A	0x10	data2	data2 If data1[0] == 0 : HW error happened
Write		0x00	0x27	0x01	
Wait 1 [ms]					
Write	Demod.	0x00	0x10	0x01	
	System (RF)	0x10	0x26	0x00	
			0x27	0x00	
			0x28	0x00	
			0x29	0x00	

5.1.4. Tune setting1



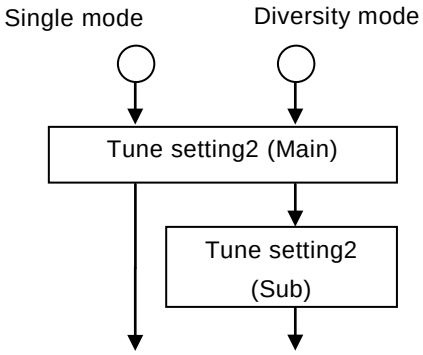
Register R/W	Slave Address	Bank	Register Address	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8
Write	Demod.	0x00	0x10	0x01							
	System (RF)	0x10	0xE7	0x00	0x00	0x0E	0x00	0x03			
			0xE7	0x1F	0x80	0x18	0x00	0x07			
Wait 1 [ms]											
Write	System (RF)	0x10	0x45	0x87	data1	0x1D	0x75	0x84	data2	0x1C	
			0x62	0x00							
		0x15	0x1E	0x03	0xE2						
		0x10	0x52	data3	0x00	0x6B	0x4D	data4	0x00	data5	data6
			0x5A	data7	0xFF	0xFE					

data1 / data2 DVB-T or ISDB-T : data1 = 0x94, data2 = 0x91 DVB-T2 : data1 = 0x96, data2 = 0x93
data3 CATV in : data3 = 0x01, Other : data3 = 0x00
data4 BW 1.7MHz : data4 = 0x03 BW 5MHz or 6MHz : data4 = 0x00 BW 7MHz : data4 = 0x01 BW8MHz : data4 = 0x02
data5 ~ data7 data5 = (uint8_t)((frequency_kHz >> 16) & 0x0F) data6 = (uint8_t)((frequency_kHz >> 8) & 0xFF) data7 = (uint8_t)(frequency_kHz & 0xFF)

5.1.5. Wait for internal CPU

Refer to initialize flow (section 4.2).

5.1.6. Tune setting2

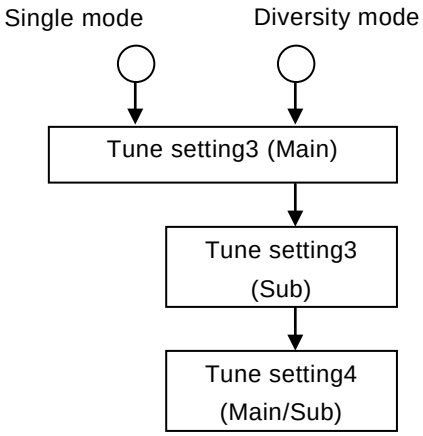


Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x11	0x2D	0x01	
			0x2E	0x0E	
			0x2F	0x01	
		0x1A	0x29	0x01	
Read			0x2C	data1	
Write		0x10	0x60	data1	Write monitored data
			0x62	0x01	
		0x11	0x2D	0x00	
			0x2F	0x00	
	Demod.	0x00	0x10	0x00	
	System (RF)	0x00	0x31	data2	data2 DVB-T : 0x01 DVB-T2 : 0x02 ISDB-T : 0x06

5.1.7. Set TS clock mode and frequency

Refer to “TS output setting” section in this document and set related registers properly.

5.2. Common tune setting2



5.2.1. Tune setting3

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0xFD	0x01	
			0xFE	0x01	
	System	0x10	0xEF	data1	data1 ~ data6 DVB-T2 & FEF control : 0x01 Other : 0x00
			0xF0	data2	
			0xF1	data3	
			0xF2	data4	
			0xF3	data5	
			0xF4	data6	
	Demod.	0x2D	0xB1	data7	data7 DVB-T2 & FEF control : 0x00 Other : 0x01

5.2.2. Tune setting4

(For diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x55	0x14	
			0x56	0x00	

(For diversity main tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0x53	0x0B	
			0x54	0xFF	
			0x57	0x01	
			0x55	0x0B	
			0x56	0xFF	

(For diversity main tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0xFE	0x01	

(For diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	System (RF)	0x00	0xFE	0x01	

5.3. DVB-T2 Tune setting

5.3.1. DVB-T2 demodulator setting

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x04	0x5D	0x0B	AGC gain setting

(This setting is NOT necessary for diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0xCE	0x01	TSIF gain setting
			0xCD	0x01	

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x20	0x8A	0x07	
			0x90	0x06	
		0x2A	0xDC	0x00	
			0xDE	0x00	
		0x2D	0x73	0x04	
			0x74	0xB0	
			0x75	0x00	
			0x76	0x00	
			0x8F	0x09	
			0x90	0x9C	
			0x91	0x0E	
			0x92	0x4C	

Register R/W	Slave Address	Bank	Register Address	CLOCKMODE_A Data	CLOCKMODE_B Data	CLOCKMODE_C Data	Description
Write	Demod.	0x04	0x1D	0x52	0x5D	0x60	
			0x1E	0x49	0x55	0x00	
			0x1F	0x2C	0x32	0x34	
			0x22	0x51	0x5C	0x5E	
			0x24	0x51	0x5C	0x5E	
			0x26	0x3D	0x45	0x47	
			0x29	0x15	0x17	0x18	
			0x2A	0x29	0x2E	0x2F	
			0x2D	0x0C	0x0D	0x0E	
			0x2E	0x04	0x05	0x05	Not necessary for diversity sub tuner
			0x2F	0xE7	0x90	0xB8	
			0x30	0x94	0x27	0xD8	
			0x31	0x92	0x55	0x00	
			0x32	0x09	0x0B	0x0B	
			0x33	0xCF	0x20	0x72	
			0x35	0x7E	0x8F	0x93	
			0x36	0xD0	0xD6	0xF3	
			0x37	0x49	0xEA	0x00	
			0x38	0xCD	0xC8	0xCD	
			0x39	0xCD	0xC8	0xCD	
			0x3A	0x1F	0x23	0x24	
			0x3B	0x5B	0x91	0x95	
			0x3C	0x0B	0x01	0x01	
			0x3D	0x6A	0x02	0x02	
			0x56	0xC9	0xE4	0xEB	
			0x57	0x03	0x03	0x03	
			0x58	0x33	0x39	0x3B	

Register R/W	Slave Address	Bank	Register Address	BW = 8MHz			BW = 7MHz			Description
				CLK mode A	CLK mode B	CLK mode C	CLK mode A	CLK mode B	CLK mode C	
Write	Demod.	0x04	0x10	0x15	0x14	0x15	0x18	0x17	0x18	
			0x11	0x00	0x6A	0x00	0x00	0x55	0x00	
			0x12	0x00	0xAA	0x00	0x00	0x55	0x00	
			0x13	0x00	0xAA	0x00	0x00	0x55	0x00	
			0x14	0x00	0xAB	0x00	0x00	0x55	0x00	
			0x15	0x00	0x00	0x00	0x00	0x00	0x00	
			0x4A	0x00	0x00	0x00	0x02	0x02	0x02	
			0x19	0x19	0x3F	0x3F	0x3F	0x3F	0x3F	
			0x1A	0xD2	0xFF	0xFF	0xFF	0xFF	0xFF	
			0x1B	0x06	0x06	0x06	0x06	0x06	0x06	
			0x1C	0x2A	0x29	0x28	0x23	0x22	0x21	
			0x4B	0x28	0x2D	0x2E	0x2D	0x33	0x35	Only for diversity main tuner
			0x4C	0x00	0x5E	0xAA	0xB6	0xDA	0x55	
			0x4D	0x50	0x5A	0x5D	0x5B	0x67	0x6A	
			0x4E	0x00	0xBD	0x55	0x6D	0xB4	0xAA	
			0x4F	0x60	0x6C	0x70	0x6D	0x7C	0x80	
			0x50	0x00	0xE3	0x00	0xB6	0x71	0x00	
			0x51	0x00	0x00	0x00	0x00	0x00	0x00	
			0x52	0x90	0xA3	0xA8	0xA4	0xBA	0xC0	
			0x53	0x00	0x55	0x00	0x92	0xAA	0x00	

Register R/W	Slave Address	Bank	Register Address	BW = 6MHz			BW = 5MHz			Description
				CLK mode A	CLK mode B	CLK mode C	CLK mode A	CLK mode B	CLK mode C	
Write	Demod.	0x04	0x10	0x1C	0x1B	0x1C	0x21	0x20	0x21	
			0x11	0x00	0x38	0x00	0x99	0xAA	0x99	
			0x12	0x00	0xE3	0x00	0x99	0xAA	0x99	
			0x13	0x00	0x8E	0x00	0x99	0xAA	0x99	
			0x14	0x00	0x39	0x00	0x9A	0xAB	0x9A	
			0x15	0x00	0x00	0x00	0x00	0x00	0x00	
			0x4A	0x04	0x04	0x04	0x06	0x06	0x06	
			0x19	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	
			0x1A	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	
			0x1B	0x06	0x06	0x06	0x06	0x06	0x06	
			0x1C	0x1C	0x1B	0x1A	0x15	0x15	0x14	
			0x4B	0x35	0x3C	0x3E	0x40	0x48	0x4A	Only for diversity main tuner
			0x4C	0x55	0x7E	0x38	0x00	0x97	0xAA	
			0x4D	0x6A	0x78	0x7C	0x6A	0x78	0x7C	
			0x4E	0xAA	0xFC	0x71	0xAA	0xFC	0x71	
			0x4F	0x80	0x91	0x95	0x80	0x91	0x95	
			0x50	0x00	0x2F	0x55	0x00	0x2F	0x55	
			0x51	0x00	0x00	0x00	0x00	0x01	0x01	
			0x52	0xC0	0xD9	0xDF	0xE6	0x05	0x0C	
			0x53	0x00	0xC7	0xFF	0x66	0x55	0xCC	

Register R/W	Slave Address	Bank	Register Address	BW = 1.7MHz						Description
				CLK mode A	CLK mode B	CLK mode C				
Write	Demod.	0x04	0x10	0x68	0x65	0x68				
			0x11	0x0F	0x2B	0x0F				
			0x12	0xA2	0xA4	0xA2				
			0x13	0x32	0xCD	0x32				
			0x14	0xCF	0xD8	0xCF				
			0x15	0x03	0x03	0x03				
			0x4A	0x03	0x03	0x03				
			0x19	0x3F	0x3F	0x3F				
			0x1A	0xFF	0xFF	0xFF				
			0x1B	0x06	0x06	0x06				
			0x1C	0x0C	0x0C	0x0B				
			0x4B	0x40	0x48	0x4A				Only for diversity main tuner
			0x4C	0x00	0x97	0xAA				
			0x4D	0x6A	0x78	0x7C				
			0x4E	0xAA	0xFC	0x71				
			0x4F	0x80	0x91	0x95				
			0x50	0x00	0x2F	0x55				
			0x51	0x02	0x03	0x03				
			0x52	0xC9	0x29	0x40				
			0x53	0x8F	0x5D	0x7D				

5.3.2. DVB-T2 set profile

Register R/W	Slave Address	Bank	Register Address	Profile			Description
				T2 BASE	T2 LITE	ANY	
Write	Demod.	0x2E	0x10	0x01	0x05	0x00	
		0x04	0x2C	data1	data2	data3	data1 CLK_A : 0x0C, CLK_B : 0x27, CLK_C : 0x27 data2 CLK_A : 0x0D, CLK_B : 0x2C, CLK_C : 0x2C data3 CLK_A : 0x0E, CLK_B : 0x2E, CLK_C : 0x2E

5.3.3. DVB-T2 PLP configuration

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x23	0xAF	data1	data1 PLP ID
			0xAD	data2	data2 Auto PLP : 0x00, Other : 0x01

5.4. DVB-T Tune setting

5.4.1. DVB-T demodulator setting

Register R/W	Slave Address	Bank	Register Address	CLOCKMODE_A Data	CLOCKMODE_B Data	CLOCKMODE_C Data	Description
Write	Demod.	0x04	0x65	0x52	0x5D	0x60	
			0x66	0x49	0x55	0x00	

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x04	0x5D	0x07	AGC gain setting

(This setting is NOT necessary for diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x00	0xCE	0x01	TSIF setting
			0xCD	0x01	

(Only for diversity mode)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x12	0x44	0x00	Diversity setting

(Only for diversity sub tuner)

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x11	0x87	0xD2	Diversity setting

Register R/W	Slave Address	Bank	Register Address	BW = 8MHz			BW = 7MHz			Description
				CLK mode A	CLK mode B	CLK mode C	CLK mode A	CLK mode B	CLK mode C	
Write	Demod.	0x04	0x68	0x73	0xC8	0xDC	0x73	0xC8	0xDC	Not necessary for diversity sub
			0x69	0xCA	0x13	0x6C	0xCA	0x13	0x6C	
			0x6A	0x49	0xAA	0x00	0x49	0xAA	0x00	
			0x60	0x15	0x14	0x15	0x18	0x17	0x18	
			0x61	0x00	0x6A	0x00	0x00	0x55	0x00	
			0x62	0x00	0xAA	0x00	0x00	0x55	0x00	
			0x63	0x00	0xAA	0x00	0x00	0x55	0x00	
			0x64	0x00	0xAA	0x00	0x00	0x55	0x00	
			0x4A	0x00	0x00	0x00	0x02	0x02	0x02	
			0x7D	0x01	0x11	0x15	0x12	0x1F	0x1F	
			0x7E	0x28	0x44	0x28	0x4C	0x15	0xF8	
			0x71	0x35	0x35	0x34	0x2F	0x2F	0x2E	
			0x4B	0x30	0x36	0x38	0x36	0x3E	0x40	Only for diversity main tuner
			0x4C	0x00	0x71	0x00	0xDB	0x38	0x00	
			0x51	0x00	0x00	0x00	0x00	0x00	0x00	
			0x52	0x90	0xA3	0xA8	0xA4	0xBA	0xC0	
			0x53	0x00	0x55	0x00	0x92	0xAA	0x00	
			0x72	0xB3	0xB3	0xB3	0xB8	0xB8	0xB8	
			0x73	0x00	0x00	0x00	0x00	0x00	0x00	
			0x6B	0x01	0x01	0x01	0x00	0x00	0x00	
			0x6C	0x02	0x02	0x02	0x03	0x03	0x03	

Register R/W	Slave Address	Bank	Register Address	BW = 6MHz			BW = 5MHz			Description
				CLK mode A	CLK mode B	CLK mode C	CLK mode A	CLK mode B	CLK mode C	
Write	Demod.	0x04	0x68	0x73	0xC8	0xDC	0x73	0xC8	0xDC	Not necessary for diversity sub
			0x69	0xCA	0x13	0x6C	0xCA	0x13	0x6C	
			0x6A	0x49	0xAA	0x00	0x49	0xAA	0x00	
			0x60	0x1C	0x1B	0x1C	0x21	0x20	0x21	
			0x61	0x00	0x38	0x00	0x99	0xAA	0x99	
			0x62	0x00	0xE3	0x00	0x99	0xAA	0x99	
			0x63	0x00	0x8E	0x00	0x99	0xAA	0x99	
			0x64	0x00	0x38	0x00	0x99	0xAA	0x99	
			0x4A	0x04	0x04	0x04	0x06	0x06	0x06	
			0x7D	0x1F	0x24	0x25	0x26	0x2B	0x2C	
			0x7E	0xF8	0x43	0x4C	0x5D	0x84	0xC2	
			0x71	0x29	0x2A	0x29	0x24	0x24	0x23	
			0x4B	0x40	0x48	0x4A	0x4C	0x57	0x59	Only for diversity main tuner
			0x4C	0x00	0x97	0xAA	0xCC	0x1C	0x99	
			0x51	0x00	0x00	0x00	0x00	0x01	0x01	
			0x52	0xC0	0xD9	0xDF	0xE6	0x05	0x0C	
			0x53	0x00	0xC7	0xFF	0x66	0x55	0xCC	
			0x72	0xBE	0xBE	0xBE	0xC8	0xC8	0xC8	
			0x73	0xAB	0xAB	0xAB	0x01	0x01	0x01	
			0x6B	0x00	0x00	0x00	0x00	0x00	0x00	
			0x6C	0x03	0x03	0x03	0x03	0x03	0x03	

5.4.2. DVB-T set profile

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod.	0x10	0x67	data1	data1 HP : 0x00 LP : 0x01

5.5. ISDB-T Tune setting

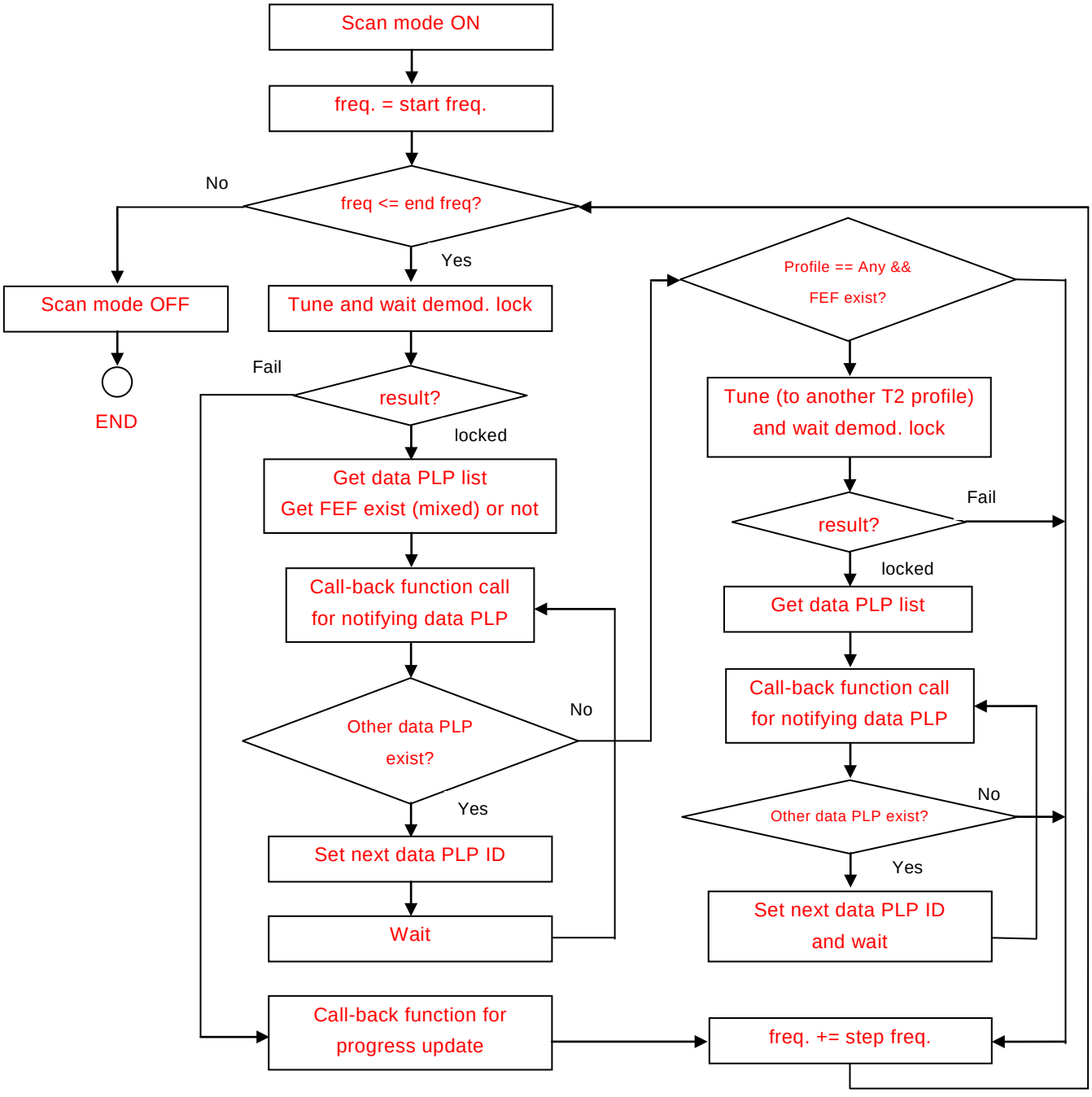
T.B.D.

6. Channel Scan

This chapter shows channel scanning flow example. Note that these examples are not enough for almost all users because these functions control tuner/demod only. Normal TV system scanning need to de-mux TS data and get many information included in TS. But they will be helpful for reference to implement scanning in user's system.

6.1. DVB-T2 Channel scan

Following shows DVB-T2 channel scanning flow example.



Note that DVB-T2 scanning algorithm is more complicated than DVB-T and ISDB-T. It's because DVB-T2 specification includes multiple PLP and T2 profile. In following chart, host processor will not wait TS lock but wait demodulation lock. If locked successfully, gets data PLP ID list included in L1 post information and switches to all data PLPs and calls call-back function.

6.1.1. Tune

- **Tune setting**

Refer to chapter 5. and set appropriate DVB-T2 reception setting.

- **Wait demodulator lock**

Check demodulator lock status using demod. lock indication register described in section 7.1.3. with polling process.
In our reference driver code, 3.5[sec] polling timeout is set for DVB-T2-base channels, 5.0[sec] timeout is set for DVB-T2-Lite channels.

- **Wait L1 post lock**

Check L1 post valid signal using L1 post status indication register described in section 7.1.4. with polling process. In our reference driver code, 300[ms] polling timeout is set for this checking loop.

6.1.2. Get data PLP ID information and call-back

- **Getting PLP list and FEF mixed information**

If locked successfully at tune process, Obtain the T2 PLP list from Data PLP monitor (described in section 7.1.13) and FEF mixed information from L1 Information (described in section 7.1.5).

- **Call-back function call to notify finding data PLP**

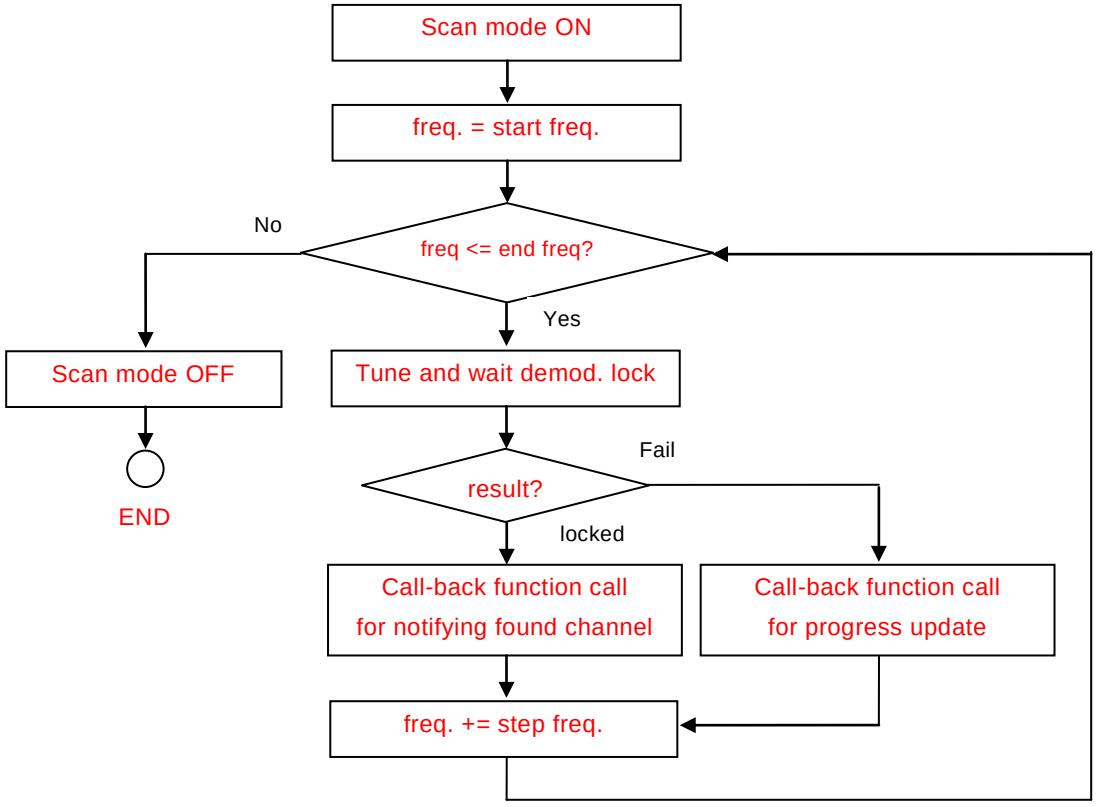
Set first PLP ID in tune parameter structure and call the scan call-back function to notify finding data PLP. After that, switches to all data PLPs and calls call-back function. To switch data PLP ID, writing register (Register address 0xAF of Bank 0x23, See also section 5.3.3) and some wait time are needed. The waiting time depends on T2 profile and FEF existence. (No FEF : 260ms, T2-base and FEF exists : 510ms, T2-Lite and FEF exists : 1260ms)

6.1.3. FEF exist case

If FEF exists, another T2 profile can exist in same frequency. So the driver calls tuning function again to try another T2 profile. If locked successfully, same as first T2 profile case, the driver get data PLP ID list and switches all data PLPs and calls call-back function.

6.2. DVB-T/ISDB-T Channel scan

Following shows DVB-T and ISDB-T channel scanning flow example.



DVB-T and ISDB-T scan function implementation is very simple. Just tune every frequency between start frequency and end frequency in specified step frequency.
Note that tune functions called from do NOT wait TS lock but demod lock. It's because user's system may want to store weak channel information that the system succeed demod lock but failed TS lock.

- **Tune setting**

Refer to chapter 5. and set appropriate DVB-T/ISDB-T reception setting.

- **Wait demodulator lock**

Check demodulator lock status using demod. lock indication register described in section 7.2.3.(for DVB-T) with polling process. In our reference driver code, 1[sec] polling timeout is set for DVB-T channels.

7. Tuner status monitor

7.1. DVB-T2 tuner and demodulator status monitor

7.1.1. Tuner RSSI

Get RSSI value.

Register R/W	Slave Address	Bank	Register Address	Data1	Data2
Write	Demod	0x00	0x10	0x01	
	System (RF)	0x10	0x5B	0x80	0x00
Wait 2 [ms]					
Read	System (RF)	0x1A	0x15	data1	data2
			0x11	data3	data4
Write	Demod	0x00	0x10	0x00	

(*) If data1 != 0 or data2 != 0, error happened.

(*) Refer to following bit allocation of 0x11(data3) and 0x12(data4) RSSI value register.

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	System (RF)	0x1A	0x11	RSSI [10:3]							
			0x12	RSSI [2:0]							

(*) RSSI value is 2's complement form.

(*) RSSI register value is in [dB] * 8.

7.1.2. Freezing / UnFreeze Registers

Function of Freeze / unfreeze monitor registers value to read them.

Freeze Registers

Register R/W	Slave Address	Bank	Register Address	Data1
Write	Demod	-	0x01	0x01

UnFreeze Registers

Register R/W	Slave Address	Bank	Register Address	Data1
Write	Demod	-	0x01	0x00

7.1.3. DVB-T2 Demod. Lock

Get demodulator lock status.

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x10			TsLock	NoOFDM		SeqState		

SeqState == 6 : Demod. Lock
SeqState != 6 : Demod. Unlock

TsLock == 1 : TS Lock
TsLock == 0: TS Unlock

NoOFDM == 1 : No Signal is detected.

7.1.4. DVB-T2 L1 Post OK

Get L1 Post valid status.

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x86								L1POST_OK

L1POST_OK == 1: L1 Post is valid
L1POST_OK == 0: L1 Post is invalid

(Notes)
- Freezing the registers setting must be set to use this function.

7.1.5. L1 Information

Get L1 information

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x1D			MIXED	MISO		FFT_SIZE		
			0x1E		GI				PP		
			0x1F				BWT_EXT	PAPR			
			0x20					NDSYM[11:8]			
			0x21	NDSYM[7:0]							

Register	meaning
MIXED	0: Not mixed, 1: Mixed
MISO	0: SISO, 1: MISO
FFT_SIZE	0: 2K, 1: 8K, 2: 4K, 3: 1K, 4: 16K, 5: 32K
GI	0: 1/32, 1: 1/16, 2: 1/8, 3: 1/4, 4: 1/128, 5: 19/128, 6: 19/256
PP	0:PP1, 1:PP2, 2:PP3, 4:PP4, 4:PP5, 5:PP6, 6:PP7, 7:PP8
BWT_EXT	0: Normal, 1: Extended
PAPR	(case: T2_VERSION == 0) 0: None, 1: ACE, 2: TR, 3: TR&ACE 4-15: Reserved (case: T2_VERSION > 0) 0: L1-ACE & P2-TR, 1: L1-ACE & ACE, 2: L1-ACE & TR, 3: L1-ACE & ACE & TR 4-15: Reserved
NDSYM[11:0]	Number of data symbols in a T2 frame

(Notes)

- The register is valid when Demod is locked.
- Freezing the registers setting must be set to use this function.

7.1.6. Carrier Frequency Offset

Get carrier frequency offset value.

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x30					CRCG_CTLVAL[27:24]			
			0x31	CRCG_CTLVAL[23:16]							
			0x32	CRCG_CTLVAL[15:8]							
			0x33	CRCG_CTLVAL[8:0]							

(Case: BandWidth 5, 6, 7, 8 MHz)
Carrier_Offset [Hz] = -1 * (CRCG_CTLVAL * (2^-30) * 8 * BW [MHz]) / (7 * 10^-6)
(Case: BandWidth 1.7 MHz)
Carrier_Offset [Hz] = -1 * (CRCG_CTLVAL * (2^-30) * 131) / (71 * 10^-6)

(Notes)
- The register is valid when Demod is locked.
- Freezing the registers setting must be set to use this function.
- CRCG_CTLVAL value is 2's compliment.

7.1.7. DVB-T2 Demodulation Information

7.1.7.1. DVB-T2 Modulation

Get Demod Modulation.

(Case: Common PLP Enable)

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0xB6	L1POST_FRAME_INTERVAL_C							
			0xB1						L1POST_PLP_MOD_C		

if L1POST_FRAME_INTERVAL_C == 0 : Error_HW_STATE happens.
Otherwise : Modulation = L1POST_PLP_MOD_C

(Case: Common PLP Disable)

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x9E						L1POST_PLP_MOD		

Modulation = L1POST_PLP_MOD

Register	meaning
L1POST_PLP_MOD	0: QPSK, 1: 16QAM, 2: 64QAM, 3: 256QAM

(Notes)

- The register is valid when L1POST_OK == 1
- Freezing the registers setting must be set to use this function.

7.1.7.2. DVB-T2 Code Rate

Get Demod Code Rate

(Case: Common PLP Enable)

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0xB6	L1POST_FRAME_INTERVAL_C							
			0xB0						L1POST_PLP_COD_C		

if L1POST_FRAME_INTERVAL_C == 0 : Error_HW_STATE happens
Otherwise : CodeRate = L1POST_PLP_COD_C

(Case: Common PLP Disable)

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x9D						L1POST_PLP_COD		

CodeRate = L1POST_PLP_COD

Register	meaning
L1POST_PLP_COD	0: 1/2, 1: 3/5, 2: 2/3, 3: 3/4, 4: 4/5 (T2Base), 5: 5/6 (T2Base)

(Notes)

- The register is valid when L1POST_OK == 1
- Freezing the registers setting must be set to use this function.

7.1.8. DVB-T2 SNR

Get SNR value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x13	snr[15:8]							
			0x14	snr[7:0]							

If snr > 10876 : snr = 10876

SNR_Value [dB] = 10* log10{ snr / (12600 – snr) } + 32.0

(Notes)

- The register is valid when Demod is locked.
- Freezing the registers setting must be set to use this function.

7.1.9. DVB-T2 Pre BCH BER

Get Pre BCH BER value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x15		BBER_VALID	BITERR[21:16]					
			0x16	BITERR[15:8]							
			0x17	BITERR[7:0]							

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0xA0							FEC_TYPE	
			0x9D						PLP_COD		

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x20	0x72					BBER_MES			

BER = BITERR / (2^(BBER_MES) * n_bch)

n_bch values are as follows.

FEC TYPE	code rate							
	1/2	3/5	2/3	3/4	4/5	5/6	1/3	2/5
16K	7200	9720	10800	11880	12600	13320	5400	6480
64K	32400	38880	43200	48600	51840	54000	21600	25920

(Notes)

- The register is valid when BBER_VALID == 1
- Freezing the registers setting must be set to use this function.

7.1.10. DVB-T2 Post BCH FER

Get Post BCH FER value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x1B	BBER_VALID	FBERR[14:8]						
			0x1C	FBERR[7:0]							
		0x20	0x72					MES[3:0]			

FER = FBERR[14:0] / (2 ^ MES[3:0])

(Notes)
- The register is valid when BBER_VALID == 1

7.1.11. DVB-T2 SSI

Get SSI value

1. Get Tuner RSSI
2. Get Modulation and Code Rate Information

prel1000 = RfLeveldBm_x1000 – ref_dbm1000

ref_dbm1000 values are as follows.

Modulation	code rate							
	1/2	3/5	2/3	3/4	4/5	5/6	1/3	2/5
QPSK	-96000	-95000	-94000	-93000	-92000	-92000	-98000	-97000
16QAM	-91000	-89000	-88000	-87000	-86000	-86000	-93000	-92000
64QAM	-86000	-85000	-83000	-82000	-81000	-80000	-89000	-88000
256QAM	-82000	-80000	-78000	-76000	-75000	-74000	-86000	-84000

- prel1000 < -15000 : SSI = 0;
- -15000 <= prel1000 < 0 : SSI = ((2 * (prel + 15000)) + 1500) / 3000
- 0 <= prel1000 < 20000 : SSI = (((4 * prel) + 500) / 1000) + 10
- 20000 <= prel1000 < 35000 : SSI = (((2 * (prel – 20000)) + 1500) / 3000) + 90
- 35000 <= prel1000 : SSI = 100

(Notes)
- If SSI > 100, set SSI = 100

7.1.12. DVB-T2 SQI

Get SQI value.

1. Get Modulation and Code Rate Information
2. Get Pre BCH BER
3. Get SNR

- BER > 10 ^ -4 : BerSQI1000 = 0
- 10 ^ -7 < BER <= 10^-3 : BerSQI1000 = 6667
- 10^-3 < BER : BerSQI1000 = 16667

snRel1000 = sn1000 – nordig_P1_dB1000

nordig_P1_dB1000 values are as follows.

Modulation	code rate							
	1/2	3/5	2/3	3/4	4/5	5/6	1/3	2/5
QPSK	3500	4700	5600	6600	7200	7700	1300	2200
16QAM	8700	10100	11400	12500	13300	13800	6000	7200
64QAM	13000	14800	16200	17700	18700	19400	9800	11100
256QAM	17000	19400	20800	22900	24300	25100	13200	14800

- SnRel1000 < -3 * 1000 : Quality = 0
- -3 * 1000 <= SnRel1000 <= 3 * 1000 : Quality = (((SnRel1000 + 3 * 10000) * BerSQI1000) + 500000) / 1000000
- 3 * 1000 < SnRel1000 : Quality = (BerSQI1000 + 500) / 1000

(Notes)

- The register is valid when Demod is locked
- If Quality> 100, set Quality = 100

7.1.13. PLP ID

Get the list and number of PLP-ID including TS frame. This function consists of the following sub-functions :

- Get the number of PLP ID including TS frame.
- Get the list of PLP ID including TS frame.

7.1.13.1. The number of PLP ID

Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	Demod	0x0B	0xC1	data1	data1 The number of PLP including TS frame

(Notes)

- The registers are valid when IL1POST_OK == 1.
- Freezing the registers setting must be set to use this function.

7.1.13.2. The list of PLP ID

Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	Demod	0x0B	0xC2	plpid000	1st PLP ID including TS frame
		0x0B	0xC3	plpid001	2nd PLP ID including TS frame
				:	
Read	Demod	0x0B	0xFE	plpid60	
		0x0B	0xFF	plpid61	
		0x0C	0x10	plpid62	
		0x0C	0x11	plpid63	
				:	
Read	Demod	0x0C	0xCF	plpid253	254th PLP ID including TS frame
		0x0C	0xD0	plpid254	255th PLP ID including TS frame

(Notes)
- The registers are valid when IL1POST_OK == 1.
- Freezing the registers setting must be set to use this function.

7.1.14. PLP SEL ERR

Checking If the selected PLP_ID was found.

Register R/W	Slave Address	Bank	Register Address	Data	Description
Read	Demod	0x0B	0xC0	data1	PLP_SEL_ERR = data1[0] PLP_SEL_ERR = 1 : Selected PLP_ID is not found. PLP_SEL_ERR = 0 : Selected PLP_ID is found.

If the selected PLP_ID is not found, the demodulator has automatically selected the first found data PLP in the channel.

(Notes)
- The registers are valid when IL1POST_OK == 1.

7.1.15. DVB-T2 PER

Get DVB-T2 PER value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0B	0x18								PER_VALID
			0x19	PKTERR[15:8]							
			0x1A	PKTERR[7:0]							

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x24	0xDC					MES[3:0]			

PER = PKTERR[15:0] / (2 ^ MES[3:0])

(Notes)

- The register is valid when PER_VALID == 1

7.2. DVB-T tuner and demodulator status monitor

7.2.1. Tuner RSSI

Get RSSI value.

It is same as DVB-T2 Tuner RSSI. Refer to section (7.1.1).

7.2.2. Freezing / UnFreeze Registers

Freeze / unfreeze monitor registers to read them

It is same as DVB-T2 Tuner Freezing/Unfreezing registers. refer to section (7.1.2).

7.2.3. DVB-T Demod. Lock

Get demodulator lock status.

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0D	0x10			TsLock	NoOFDM		SeqState		

SeqState == 6 : Demod. Lock
SeqState != 6 : Demod. Unlock

TsLock == 1 : TS Lock
TsLock == 0: TS Unlock

NoOFDM == 1 : No Signal is detected.

7.2.4. DVB-T TPS Information

Get Demod lock status

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0D	0x29	CNST[1:0]		HIER[2:0]			HRATE[2:0]		
			0x2A	LRATE[2:0]			GI[1:0]		MODE[1:0]		
			0x2B	FNUM[1:0]		LENGTH_INDICATOR[5:0]					
			0x2C	CELLID[15:8]							
			0x2D	CELLID[7:0]							
			0x2E			RESERVE_EVEN[5:0]					
			0x2F			RESERVE_ODD[5:0]					
		0x11	0xD5								CELLID_OK

Register	meaning
CNST[1:0]	0: QPSK, 1: 16QAM, 2: 64QAM 3: Reserved
HIER[2:0]	0: non -hierarchical service 1: α=1, 2: α=2, 3: α=4
HRATE[2:0]	0: 1/2, 1: 2/3, 2: 3/4, 3: 5/6, 4: 7/8 5-7: Reserved
LRATE[2:0]	
GI[1:0]	0: 1/32, 1: 1/16, 2: 1/8, 3: 1/4
MODE[1:0]	0: 2K, 1: 8K, 2-3: Reserved
FNUM[1:0]	Frame number in the super-frame 0: number 1, 1: number 2, 2: number 3, 3: number 4
LENGTH_ INDICATOR[5:0]	TSP length indicator
CELLID[15:0]	cell Identifier
RESERVE_EVEN[5:0]	Reserved
RESERVE_ODD[5:0]	Reserved

(Notes)

- The register is valid when Demod is locked.
- Freezing the registers setting must be set to use this function.

7.2.5. Carrier Frequency Offset

Get carrier frequency offset value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0D	0x1D				CRCG_CTLVAL[28:24]				
			0x1E	CRCG_CTLVAL[23:16]							
			0x1F	CRCG_CTLVAL[15:8]							
			0x20	CRCG_CTLVAL[7:0]							

Carrier_Offset [Hz] = -1 * (CRCG_CTLVAL * (2^-28) * 8 * BW [MHz]) / (7 * 10^-6)

(Notes)
- The register is valid when Demod is locked.
- CRCG_CTLVAL is 2's compliment.
- Freezing the registers setting must be set to use this function.

7.2.6. DVB-T SNR

Get SNR value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0D	0x13	snr[15:8]							
			0x14	snr[7:0]							

If snr > 4996 : snr = 4996

SNR_Value [dB] = 10* log10{ snr / (5350 – snr) } + 28.5

(Notes)
- The register is valid when Demod is locked.
- Freezing the registers setting must be set to use this function.

7.2.7. DVB-T Pre RS BER

Get Pre RS BER value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x10	0x60				BERN_PERIOD				
		0x0D	0x15		BERN_ VALID	BERN_BITECNT[21:16]					
			0x16	BERN_BITECNT[15:8]							
			0x17	BERN_BITECNT[7:0]							

PrePSBER = BERN_BITECNT / (2^(BERN_PERIOD) * 204 * 8)

(Notes)

- The register is valid when Demod is locked.
- The register is valid when BERN_VALID == 1

7.2.8. DVB-T Post RS PER

Get Post RS PER value

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x0D	0x18								PER_ VALID
			0x19	FBERR[15:8]							
			0x1C	FBERR[7:0]							
		0x10	0x5C					PER_MES[3:0]			

PER = FBERR / (2 ^ PER_MES)

(Notes)

- The register is valid when PER_VALID == 1

7.2.9. DVB-T SSI

Get SSI value

1. Get Tuner RSSI
2. Get TPS Information

prel1000 = RfLeveldBm_x1000 – ref_dbm1000

ref_dbm1000 values are as follows.

Modulation	code rate				
	1/2	2/3	3/4	5/6	7/8
QPSK	-93000	-91000	-90000	-89000	-88000
16QAM	-87000	-85000	-84000	-83000	-82000
64QAM	-82000	-80000	-78000	-77000	-76000

- prel1000 < -15000 : SSI = 0
- -15000 <= prel1000 < 0 : SSI = ((2 * (prel + 15000)) + 1500) / 3000
- 0 <= prel1000 < 20000 : SSI = (((4 * prel) + 500) / 1000) + 10
- 20000 <= prel1000 < 35000 : SSI = (((2 * (prel – 20000)) + 1500) / 3000) + 90
- 35000 <= prel1000 : SSI = 100

(Notes)
- The register is valid when Demod is locked.
- If SSI > 100, set SSI = 100

7.2.10. DVB-T SQI

Get SQI value

1. Get TPS Information
2. Get Hierarchy signal (If there is hierarchy. See following table)
3. Get Pre RS BER
4. Get SNR

Register R/W	Slave Address	Bank	Register Address	bit7	bit6	bit5	bit4	bit3	bit2	Bit1	bit0
Read	Demod	0x10	0x67								LPSELECT

LPSELECT == 1 : Low Profile
LPSELECT == 0 : High Profile

snRel1000 = sn1000 – nordig_DVBT_dB1000

nordig_DVBT_dB1000 (For Non Hierarchy) values are as follows.

Modulation	code rate				
	1/2	2/3	3/4	5/6	7/8
QPSK	5100	6900	7900	8900	9700
16QAM	10800	13100	14600	15600	16000
64QAM	16500	18700	20200	21600	22500

nordig_DVBT_dB1000 (For High Profile) values are as follows.

α	Modulation	code rate				
		1/2	2/3	3/4	5/6	7/8
1	16QAM	9100	12000	13600	15000	16000
	64QAM	10900	14100	15700	19400	20600
2	16QAM	6800	9100	10400	11900	12700
	64QAM	8500	11000	12800	15000	16000
4	16QAM	5800	7900	9100	10300	12100
	64QAM	8000	9300	11600	13000	12900

nordig_DVBT_dB1000 (For Low Profile) values are as follows.

α	Modulation	code rate				
		1/2	2/3	3/4	5/6	7/8
1	16QAM	12500	14300	15300	16300	16900
	64QAM	16700	19100	20900	22500	23700
2	16QAM	15000	17200	18400	19100	20100
	64QAM	18500	21200	23600	24700	25900
4	16QAM	19500	21400	22500	23700	24700
	64QAM	21900	24200	25600	26900	27800

- BER > 10 ^ -3 : BerSQI1000 = 0
- 10 ^ -7 < BER <= 10^-3 : BerSQI1000 = (20 * Log10(1/BER) – 40) *1000
- 10^-3 < BER : BerSQI1000 = 100 * 1000

- SnRel1000 < -7 * 1000 : Quality = 0
- -7 * 1000 < SnRel1000 <= 3 * 1000 :
  Quality = ((((SnRel1000 – 3 * 10000) / 10) + 1000) * BerSQI1000 + 500000) / 1000000
- 3 * 1000 < SnRel1000 : Quality = (BerSQI1000 + 500) / 1000

(Notes)

- The register is valid when Demod is locked.
- If Quality> 100, set Quality = 100

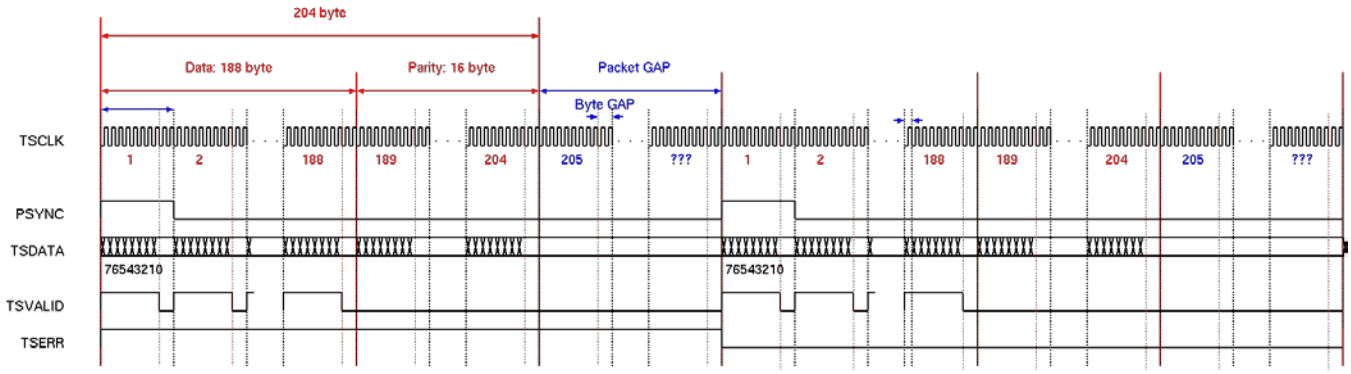
7.3. ISDB-T Demod Monitoring

T.B.D.

8. TS output setting

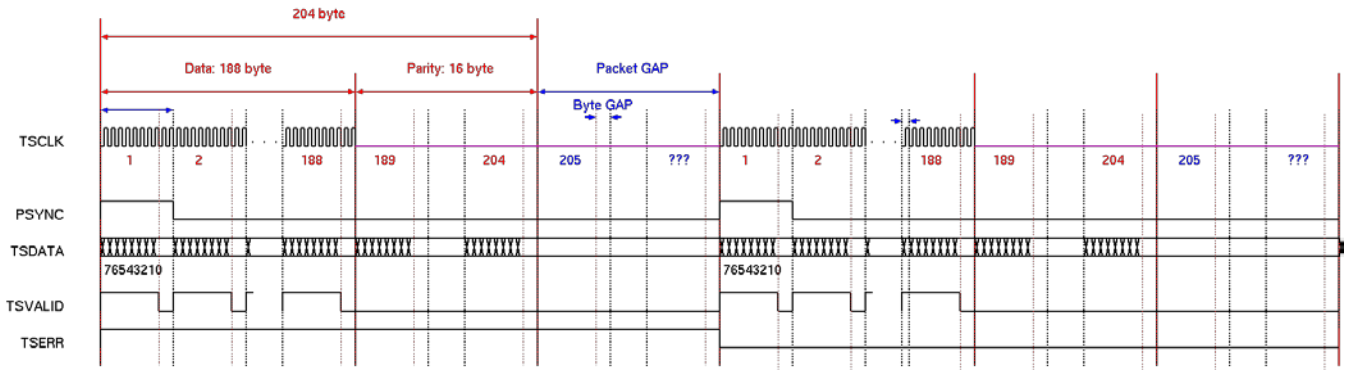
8.1. TS interface

SMT-EW10x/30x series tuner module supports DVB-SPI compliant TS output format. Following shows a typical DVB-SPI TS timing chart.

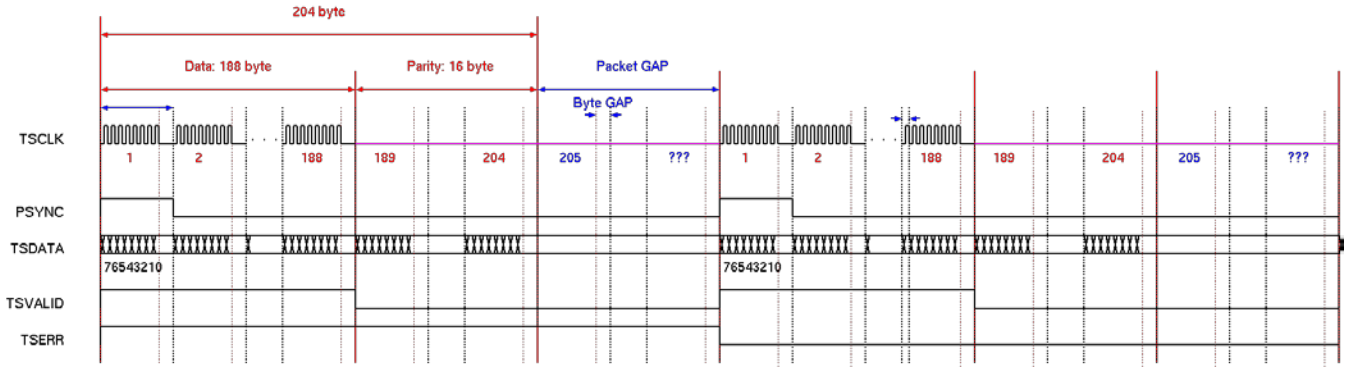


TSCLK frequency can be selected to Full-rate mode or Half-rate mode by register configuration, and also TSCLK/TVALID format, parity packet gap can be configured as following examples.

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod	0x00	0xC3	data1	data1[0] TS output control "0" : TS normal output enable "1" : TS output disable
			0xC4	dara2	data2[1:0] 00 : TS serial, Half-rate TSCLK data only mode 01 : TS serial, Full-rate TSCLK continuous mode 10 : TS serial, Half-rate TSCLK continuous mode 11 : TS serial, Full-rate TSCLK data only mode
			0xC5	data3	data3[0] TSCLK inversion setting data3[2:1] TSVALID, TSSYNC inversion setting
			0xC6	data4	data4[0] Disable TSCLK of parity and packet gap 0 : active 1 : disabled



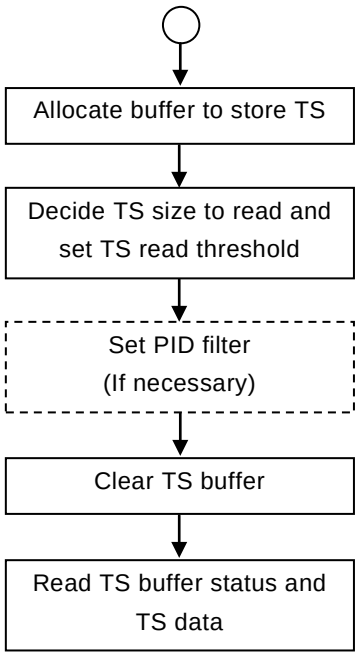
Example 1. Disable TSCLK of parity and packet gap



Example 2. Disable TSCLK of parity and packet gap

8.2. SPI interface

Following shows flow and register settings to read TS data via the SPI interface.



(Buffer status threshold setting)

Available TS buffer capacity will vary depending on reception mode. Refer to following table and set properly values to threshold registers.

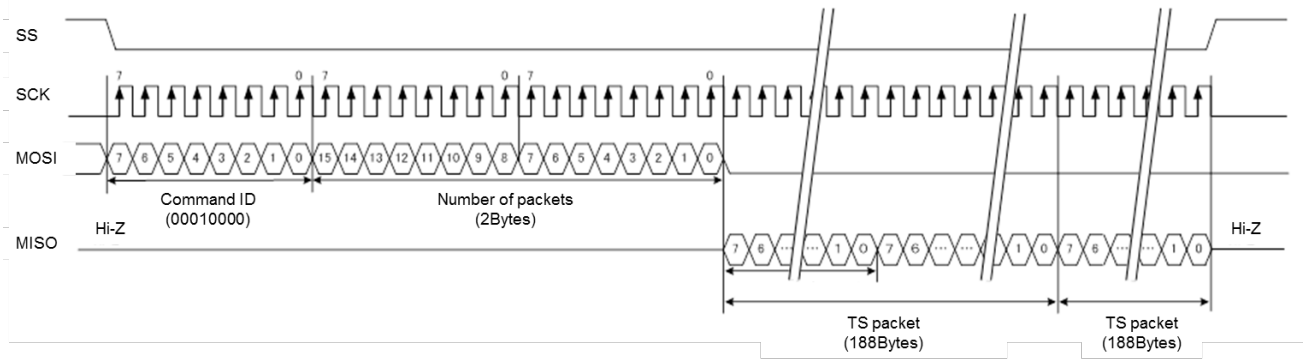
	Available threshold value		
	DVB-T2 S-PLP / M-PLP without Common	DVB-T2 S-PLP / M-PLP without Common	DVB-T / ISDB-T
Read ready	0 ~ 2008	0 ~ 837	0 ~ 1114
Almost full	2008 ~ 0	837 ~ 0	1114 ~ 0
Almost empty	0 ~ 2008	0 ~ 837	0 ~ 1114

Register R/W	Slave Address	Bank	Register Address	Data	Description
Write	Demod	0x00	0x99	data1	data1[2:0] TS buffer almost empty threshold MSB[10:8]
			0x9A	data2	data2[7:0] TS buffer almost empty threshold LSB [7:0]
			0x9B	data3	data3[2:0] TS buffer almost full threshold MSB[10:8]
			0x9C	data4	data4[7:0] TS buffer almost full threshold LSB [7:0]
			0x9D	data5	data5[2:0] TS buffer read ready threshold MSB[10:8]
			0x9E	data6	data6[7:0] TS buffer read ready threshold LSB [7:0]

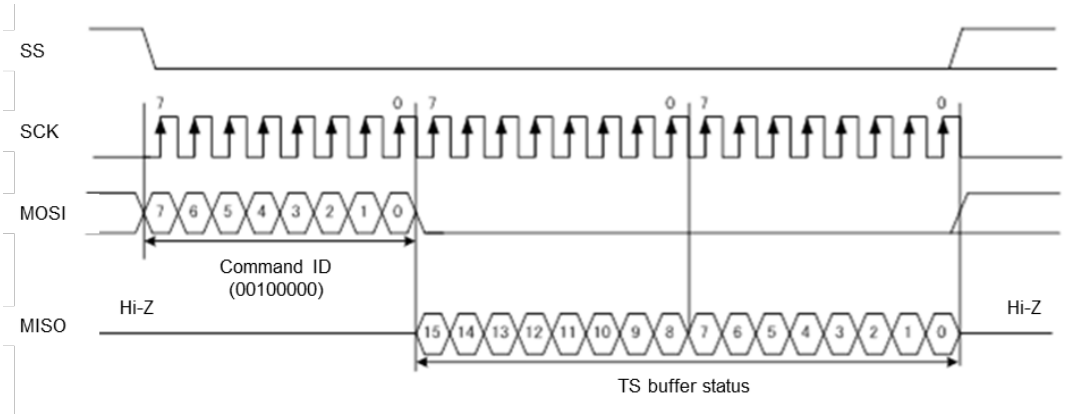
(Clear TS buffer, Read TS / Status information)

Function	Command ID	Arguments	Response	Description
Read TS	00010000	Number of read packets	TS data	Read TS data by 1packet unit
Read status	00100000	N/A	Buffer status	Read TS buffer status
Read status / TS	00110000	Number of read packets	TS data and buffer status	Read both TS buffer status and TS data
Buffer clear	00000011	N/A	N/A	Clear TS buffer

➢ Data format for reading TS packets

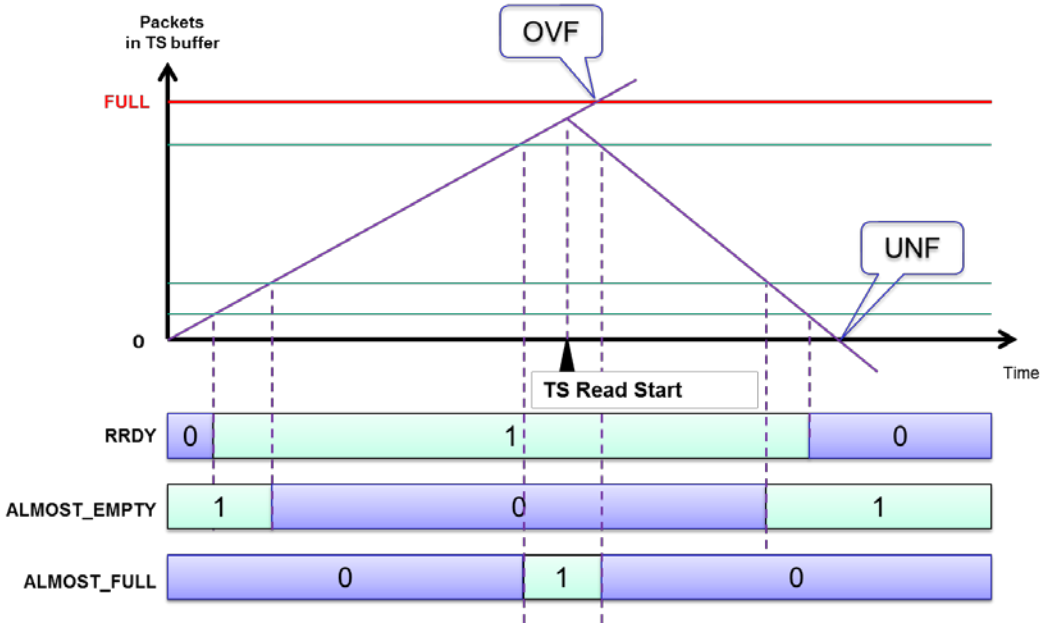


➢ Data format for reading TS buffer status

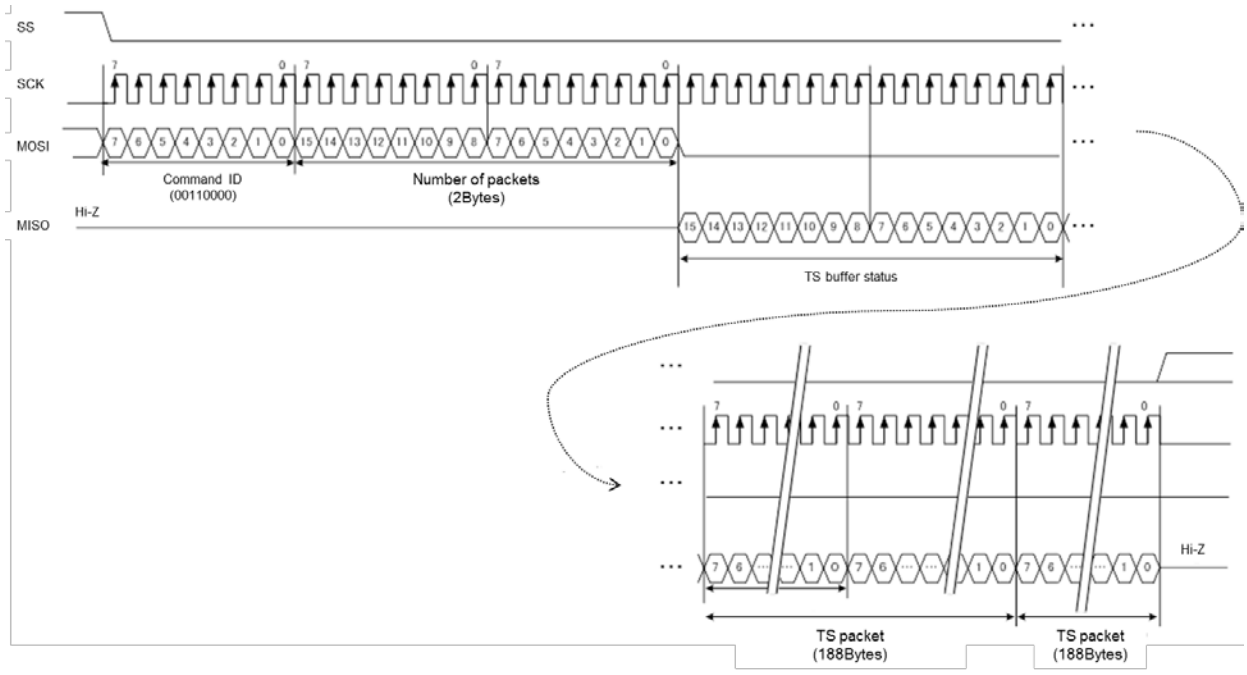


TS buffer status information

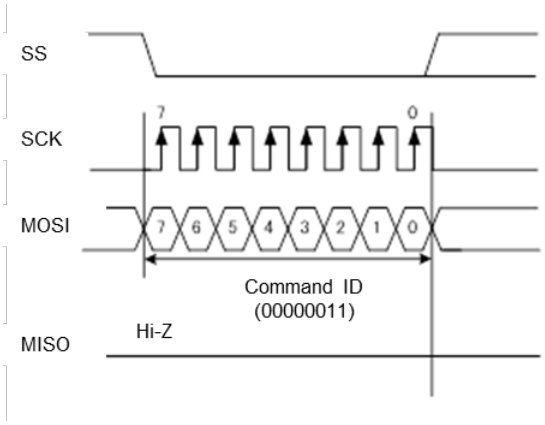
Bit	Signal	Description
[15]	BUF_RRDY	TS buffer ready flag. If this bit is 1, TS data can be read from the TS buffer.
[14]	BUF_ALMOST_FULL	TS buffer almost full flag. If this bit is 1, TS data buffer is almost full.
[13]	BUF_ALMOST_EMPTY	TS buffer almost empty flag. If this bit is 1, TS data buffer is almost empty.
[12]	BUF_OVF	TS buffer overflow flag. If this bit is 1, TS buffer overflow occurred.
[11]	BUF_UNF	TS buffer underflow flag. If this bit is 1, TS buffer underflow occurred.
[10:0]	BUF_STORED_PKT	Number of packets in TS buffer.



➢ Data format for reading TS data and buffer status



➢ Data format of TS buffer clear command



8.3. SDIO Interface

T.B.D.

9. General purpose input / output

T.B.D.

10. Interrupt function

T.B.D.